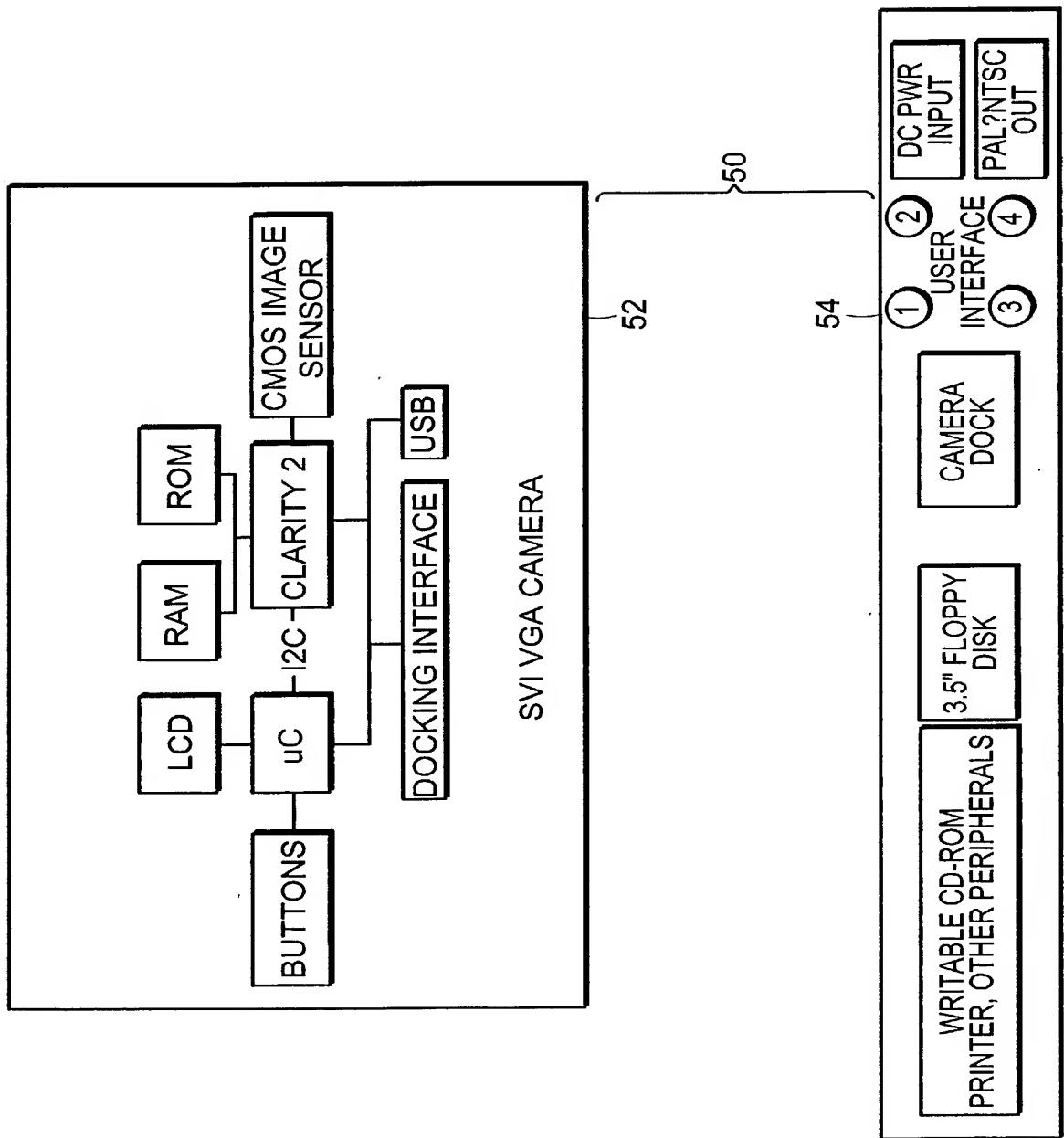
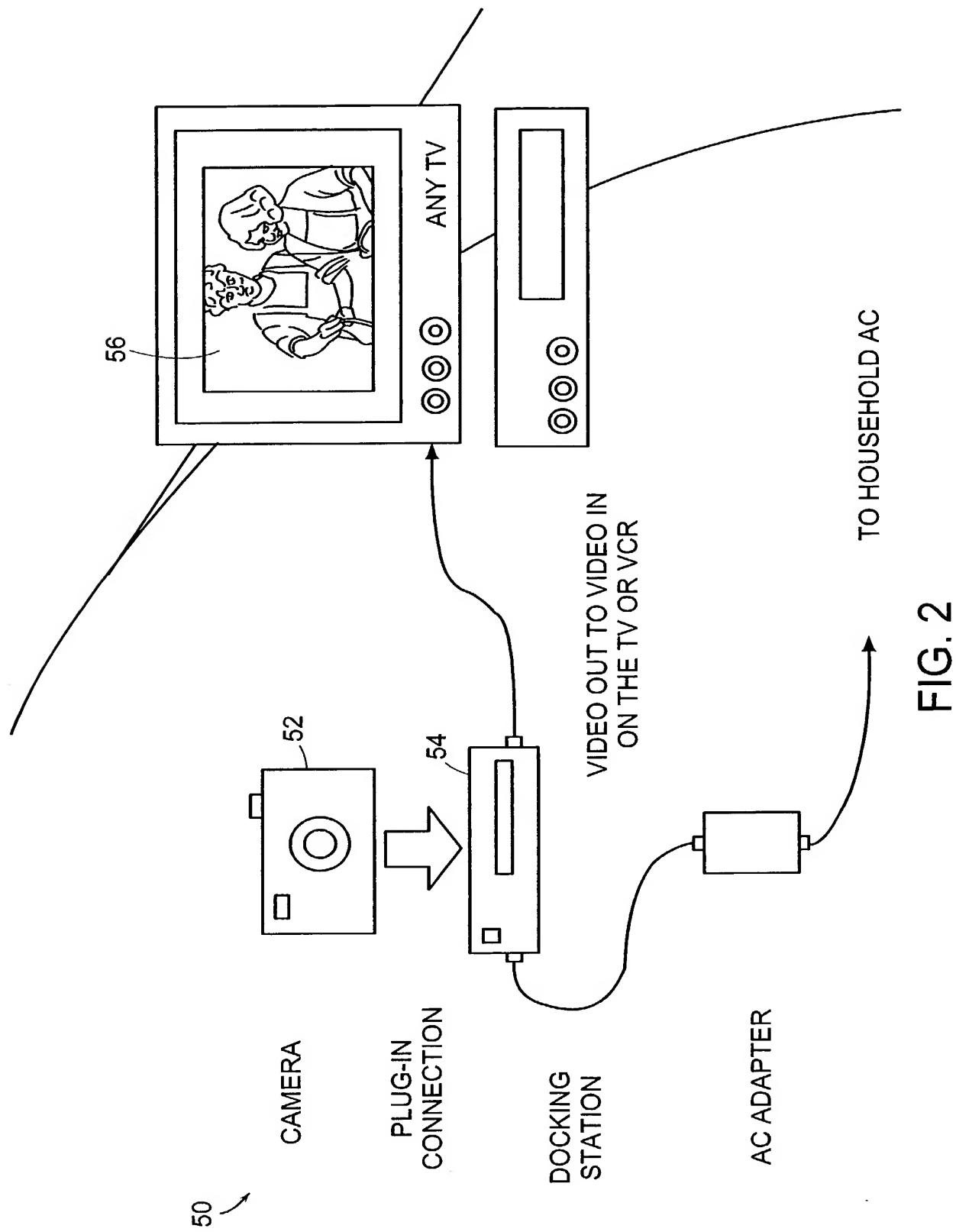
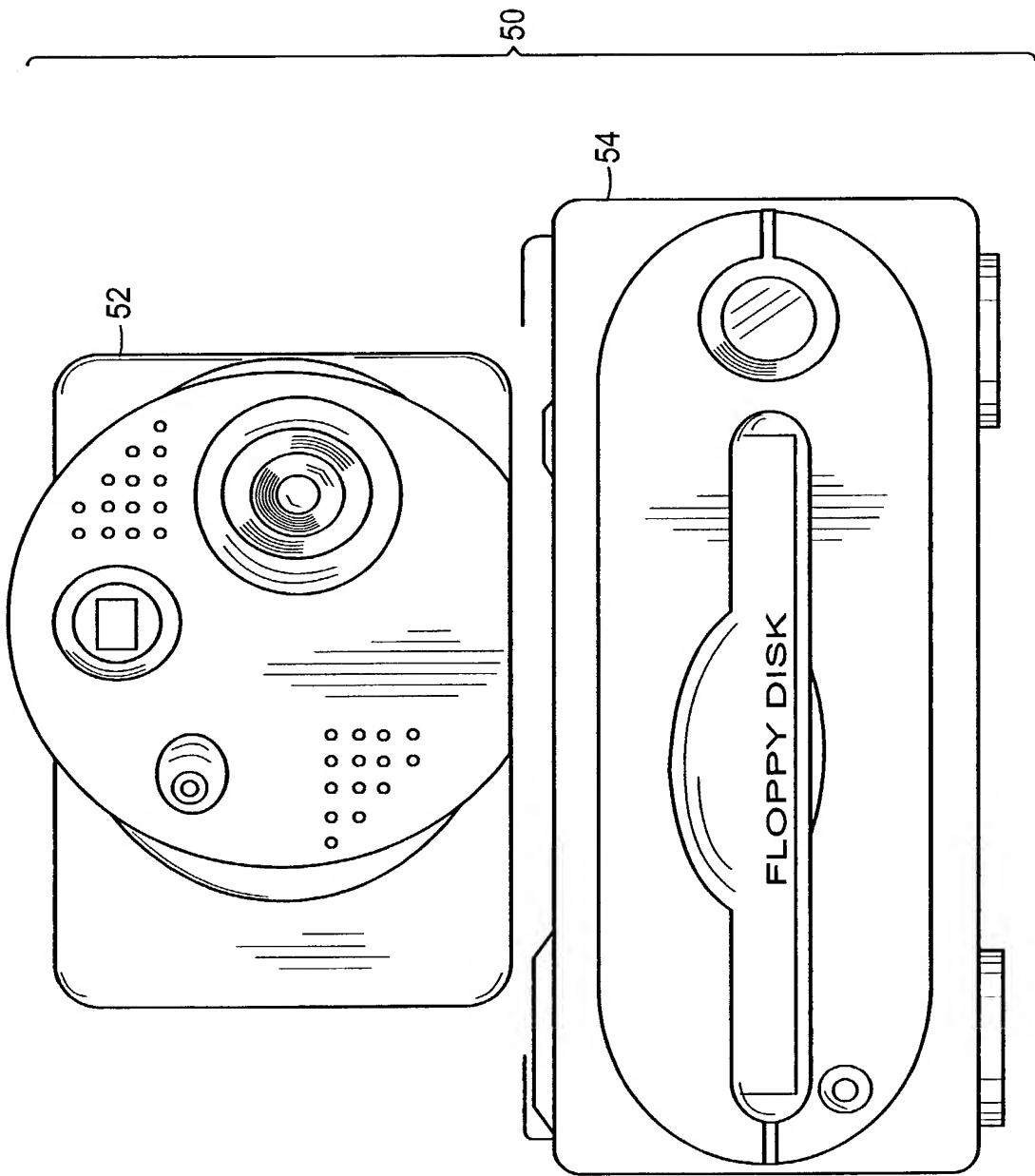


FIG. 1



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3
FIG.

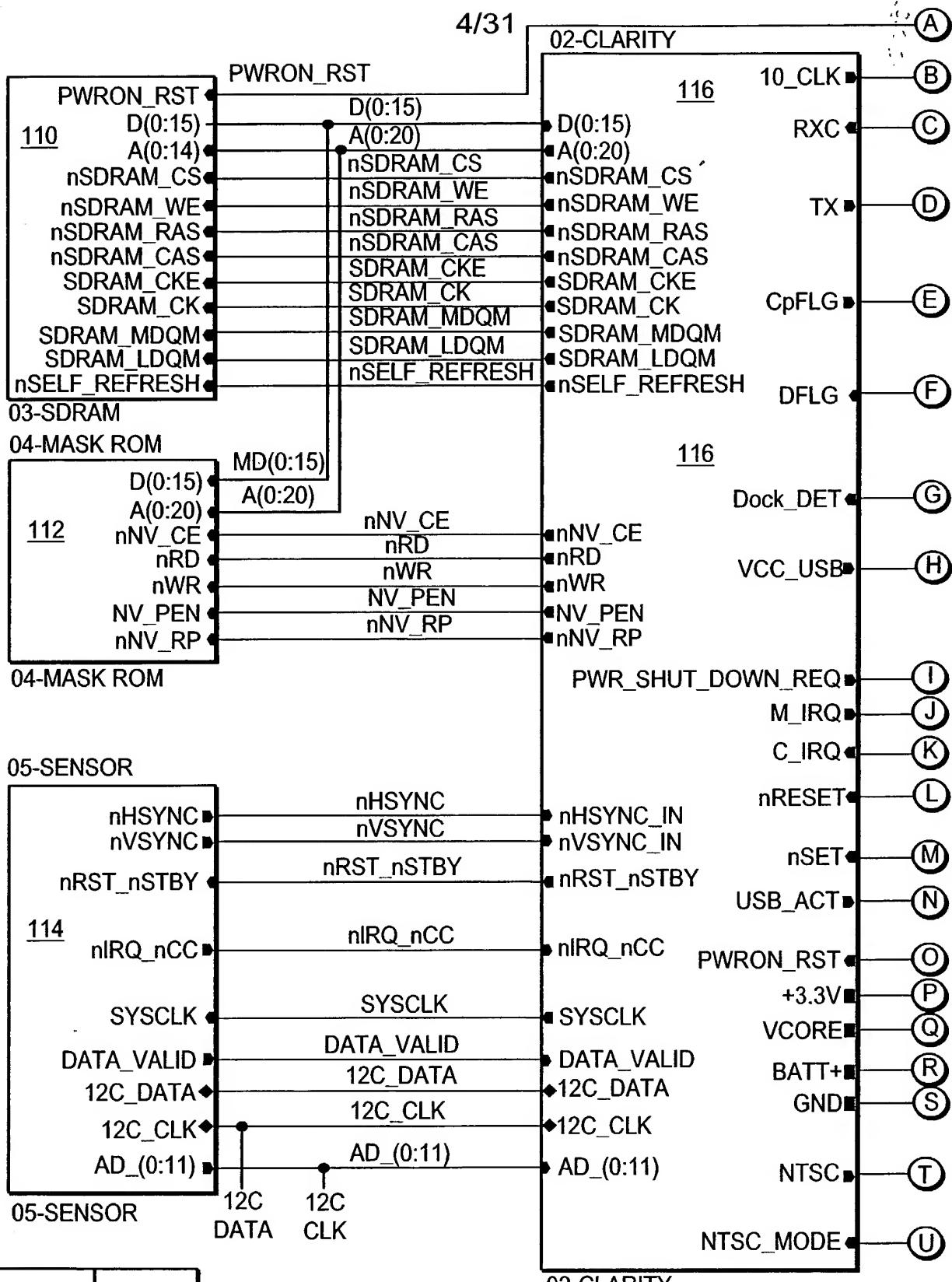
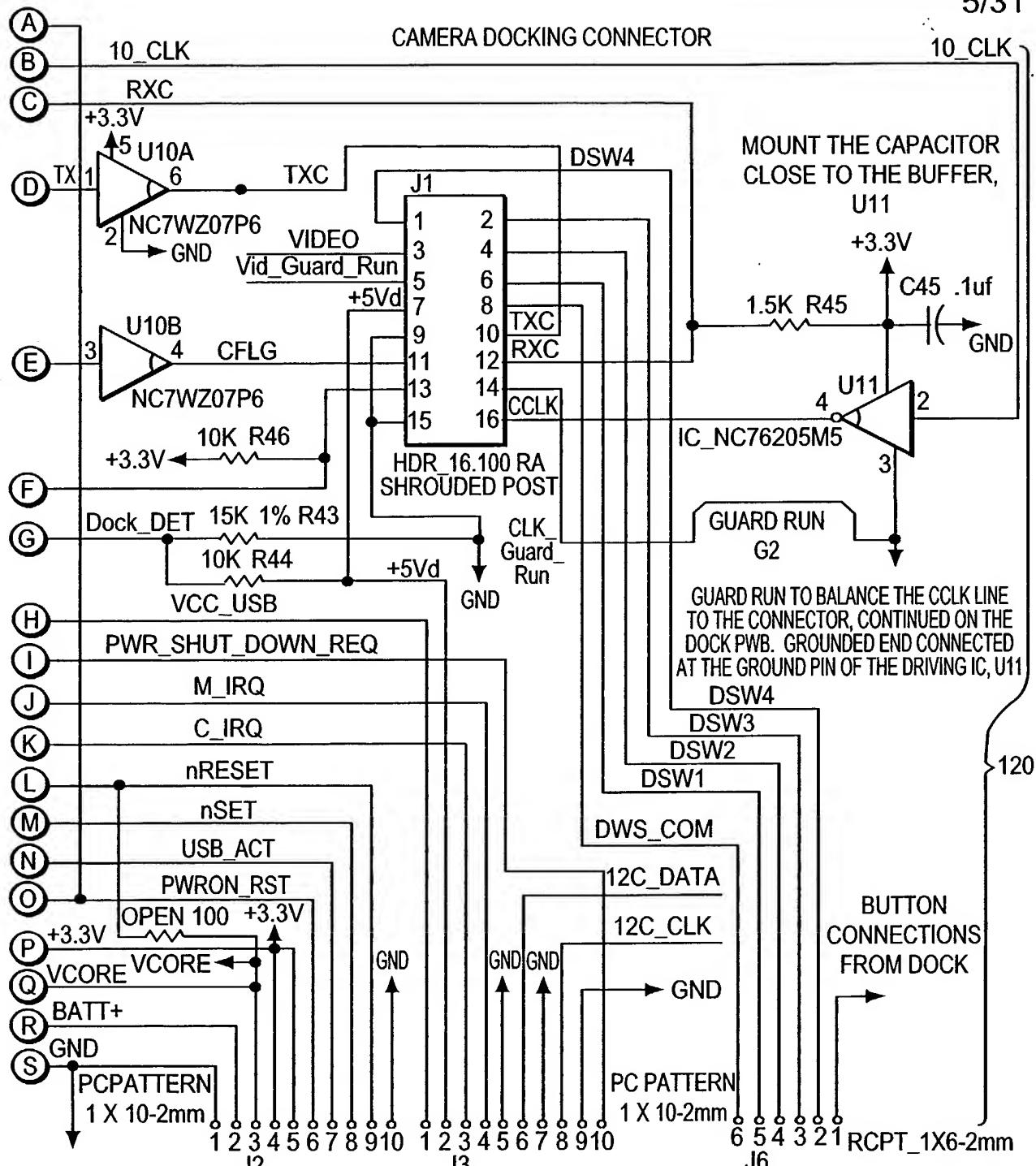


FIG. 4A

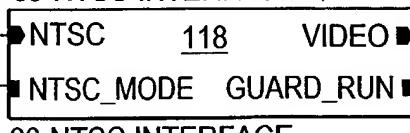
FIG. 4



USE A 10K RESISTOR AT R100
FOR DEVELOPMENT USE WITH
OLDER SV35107 AND ARM ICE.

CONNECTION TO CONTROLLER
POWER SUPPLY BOARD

09-NTSC INTERFACE



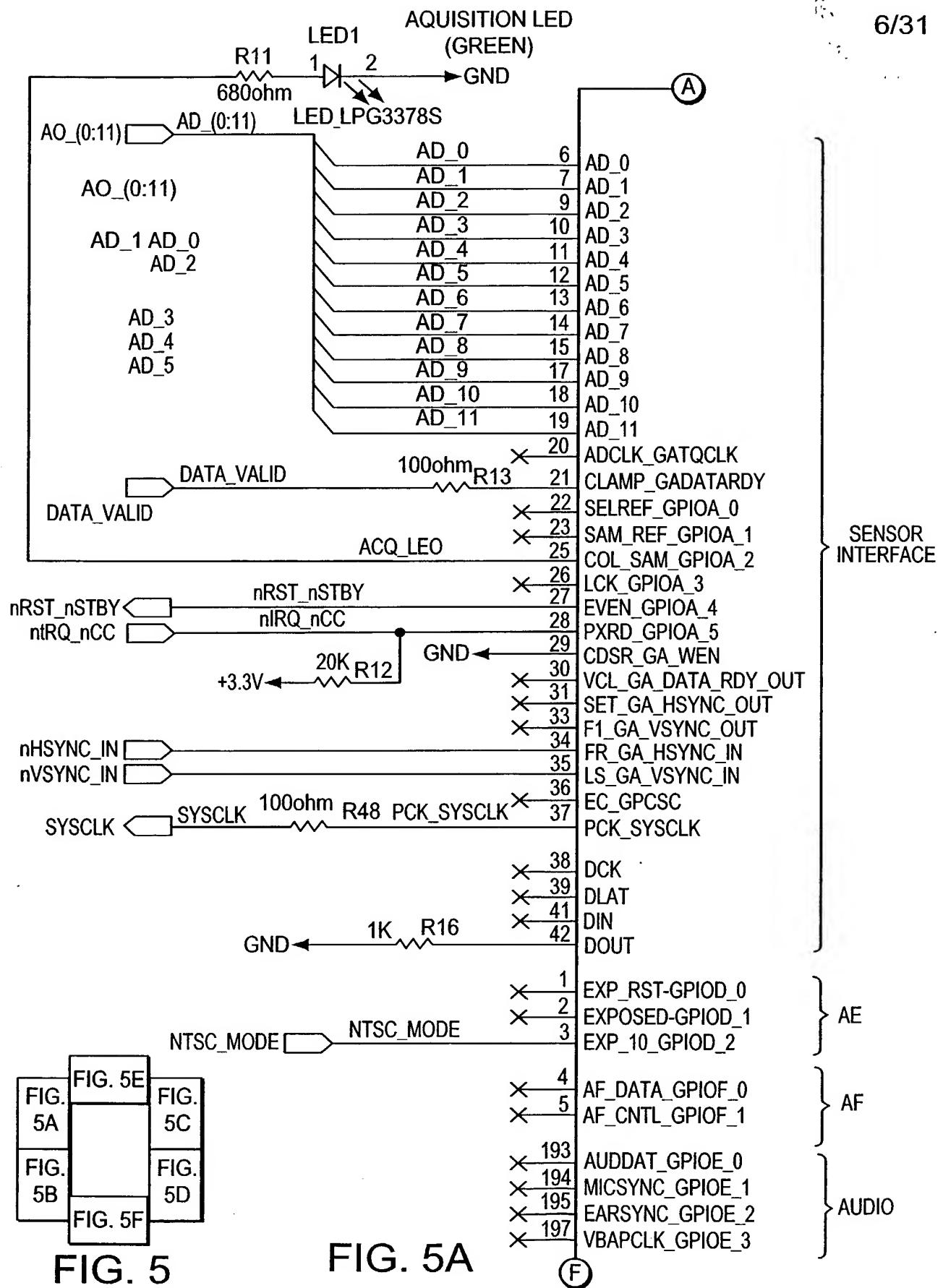
VIDEO

VID_GUARD_RUN

THE VIDEO AND THE GUARD_RUN
TRACE MUST RUN TOGETHER TO
CONTROL NOISE.

06-NTSC INTERFACE

FIG. 4B



PATTERN IS 2 ROWS OF 4 PEDS ON 0.1" CENTERS

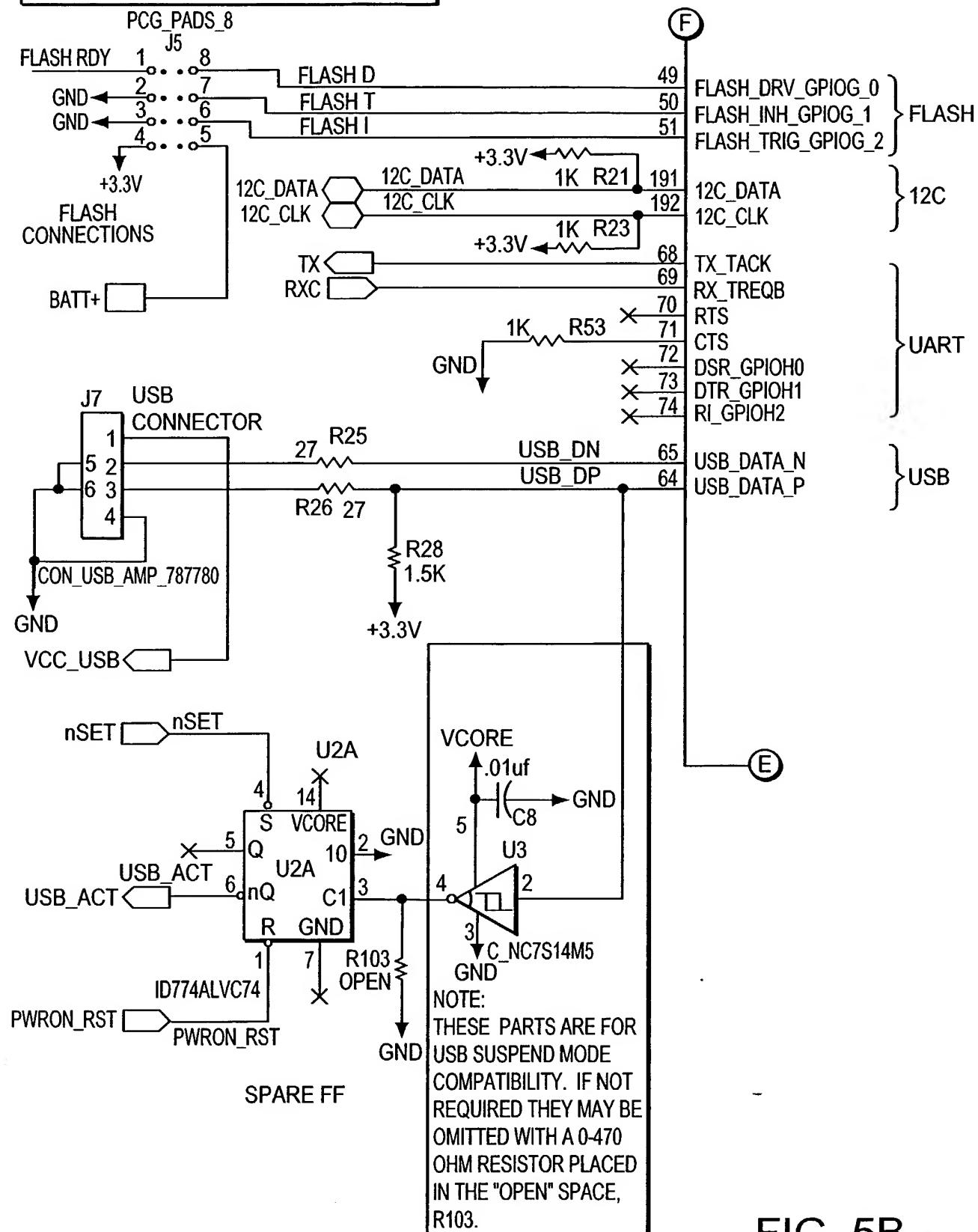


FIG. 5B

NOTE: TGND IS A PORTION OF THE GROUND PLANE PROTECTED WITH CUTS. IT IS NOT A SEPARATE RUN!

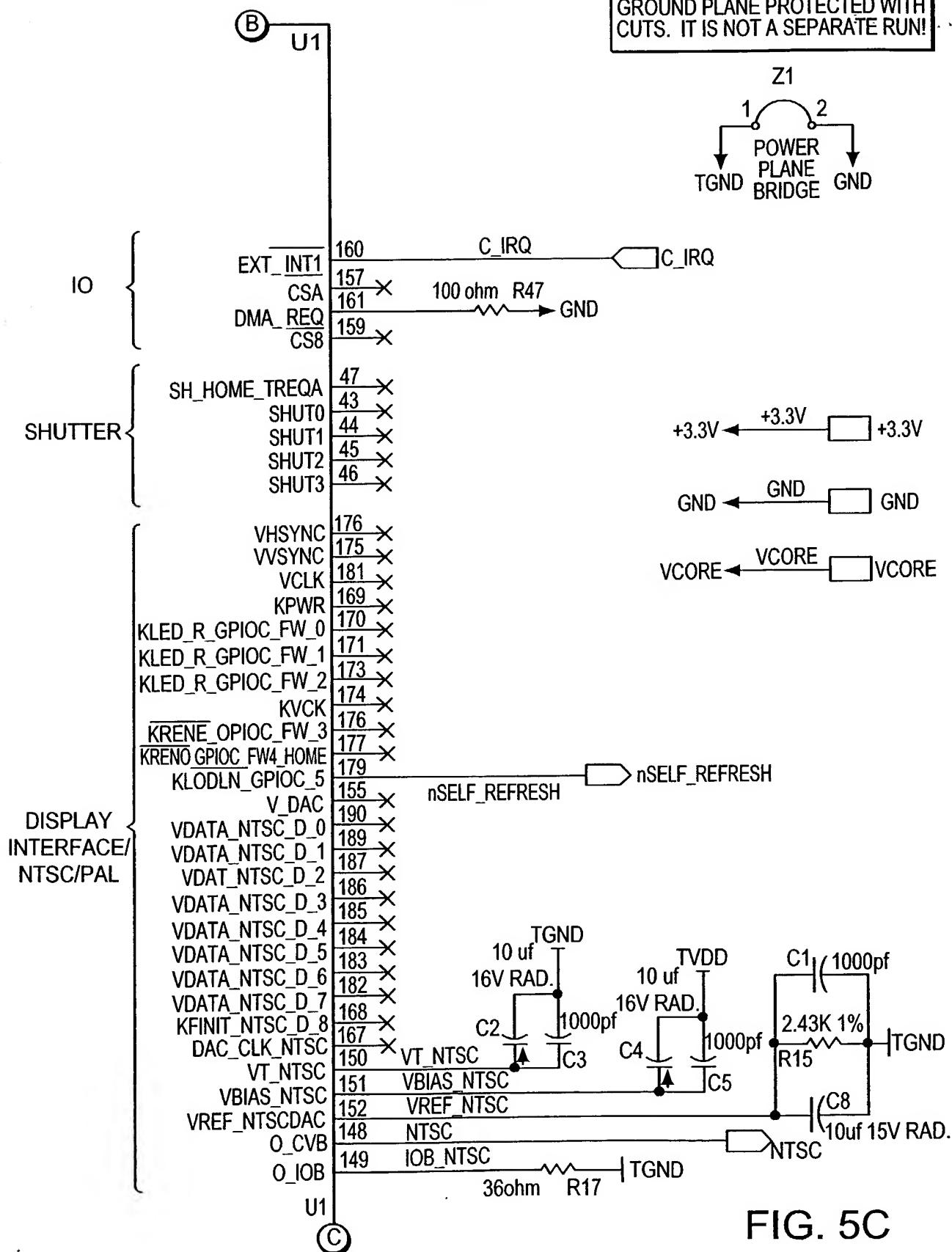


FIG. 5C

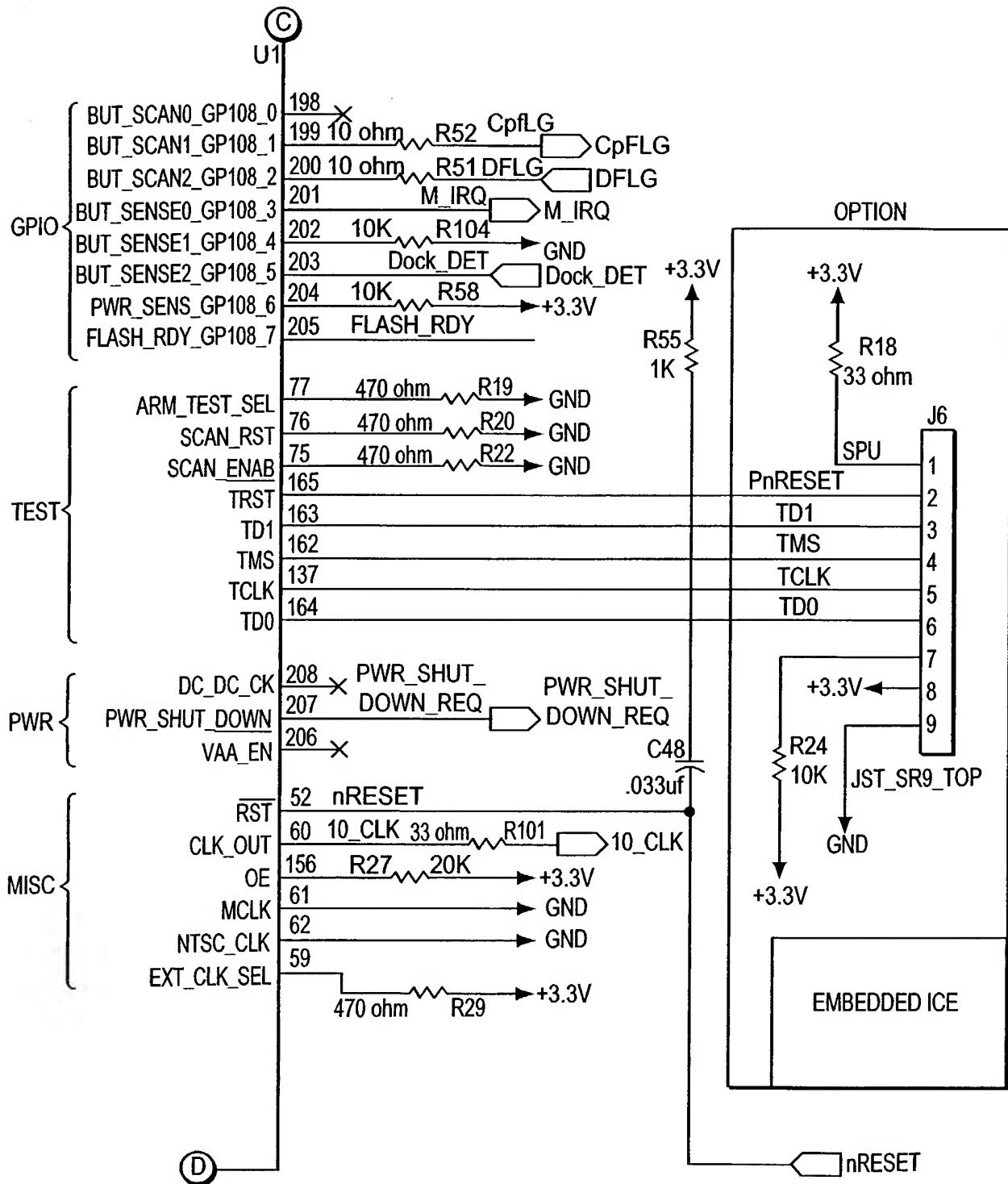


FIG. 5D

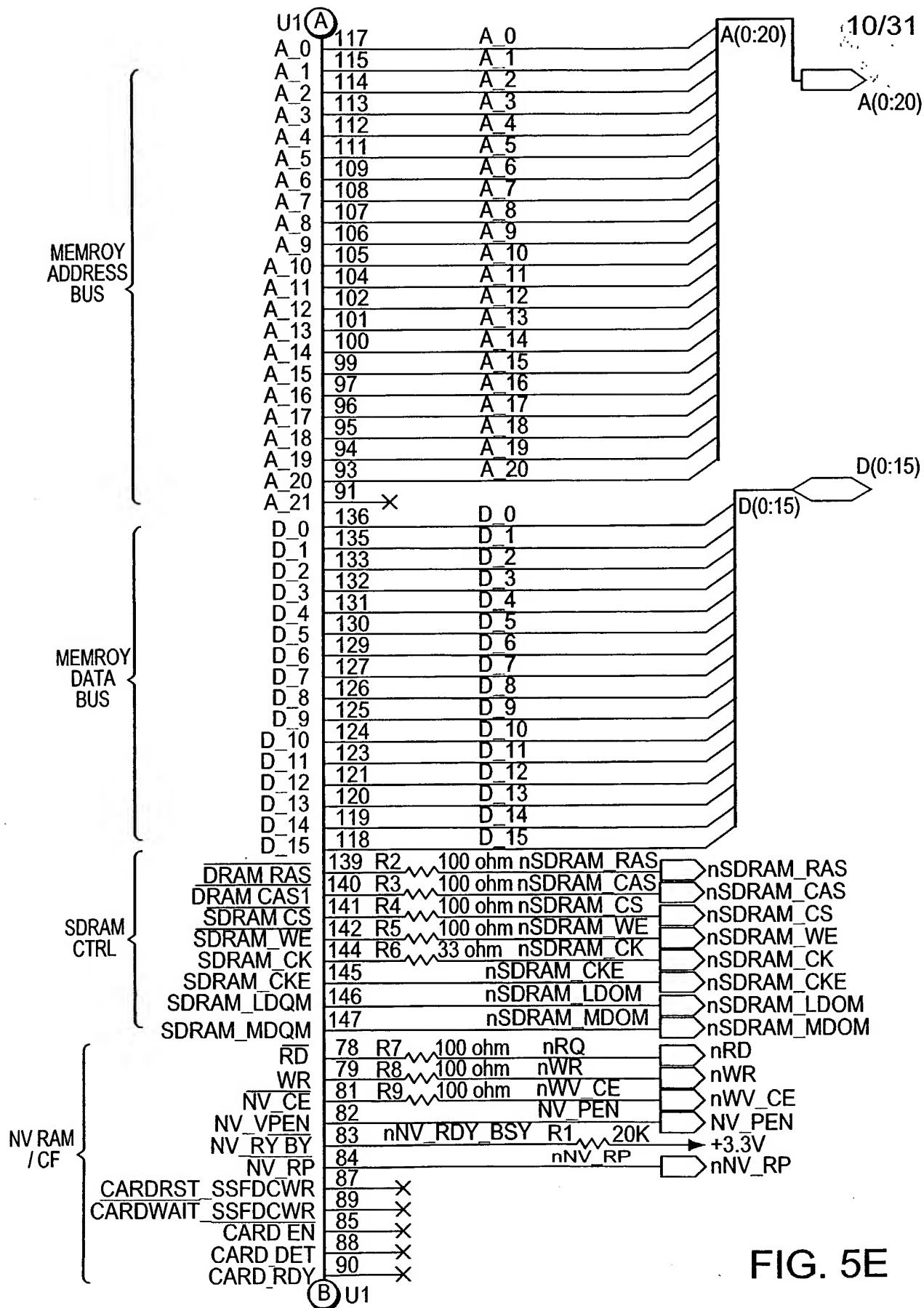


FIG. 5E

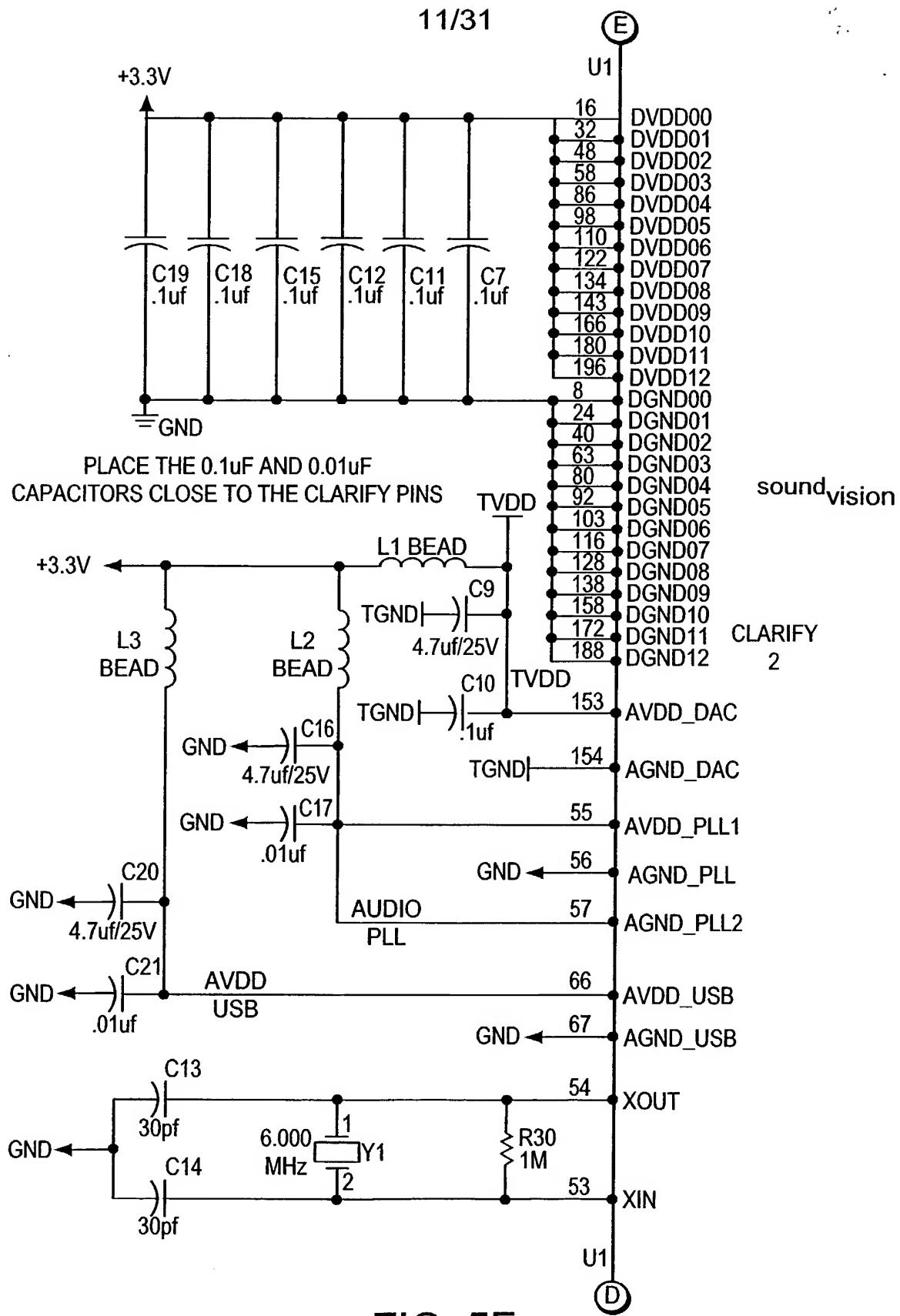


FIG. 5F

FIG. 6

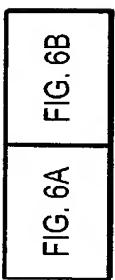
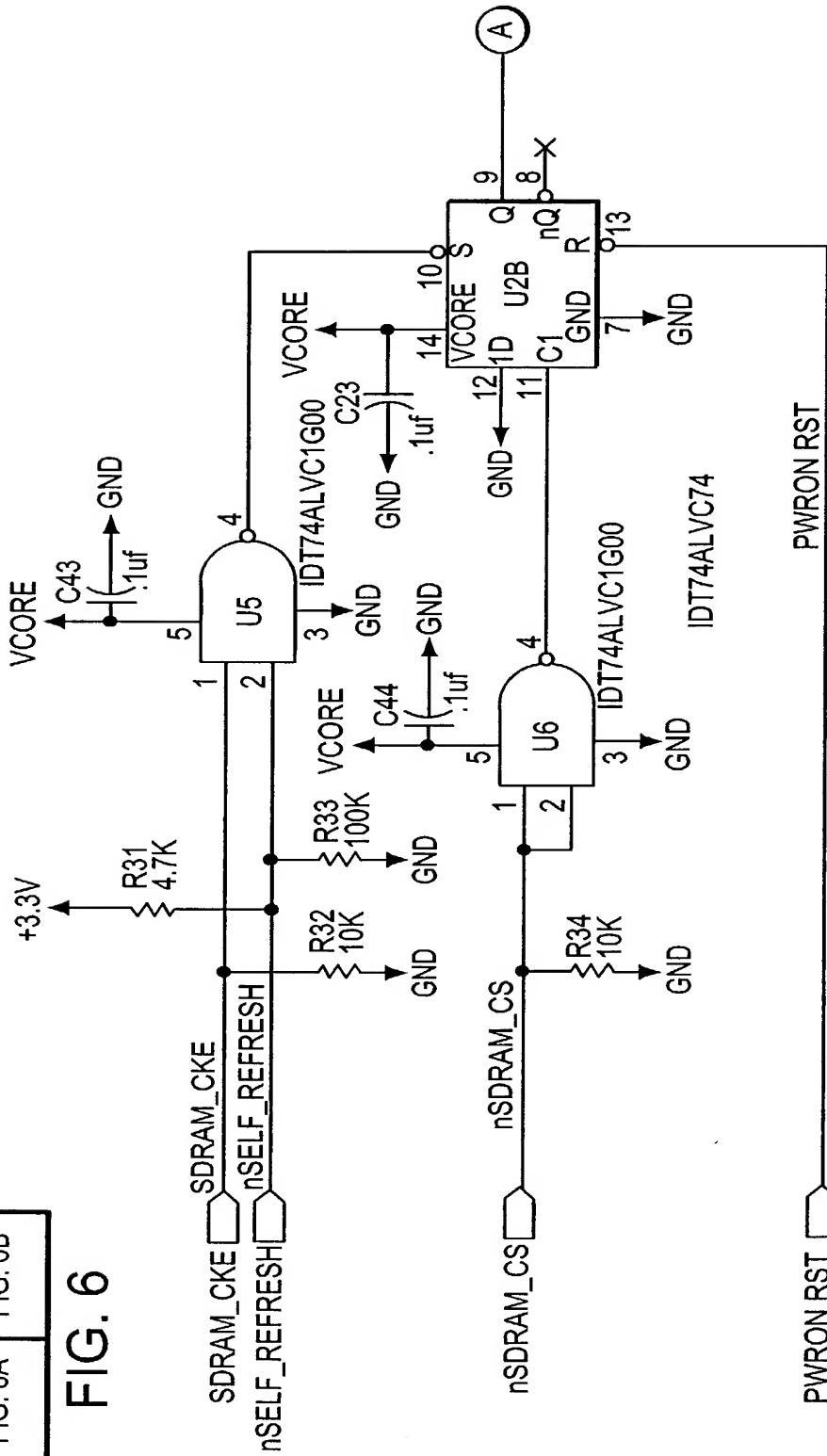


FIG. 6A FIG. 6B

FIG. 6B

FIG. 6A FIG. 6B



LOW POWER SDRAM SHOULD BE USED. POWER CONSUMPTION WHEN THE CAMERA IS SHUT DOWN DEPENDS ON THE SDRAM CONSUMPTION IN SELF REFRESH MODE AS THE MAJOR COMPONENT OF QUIESCENT CONSUMPTION.

FIG. 6A

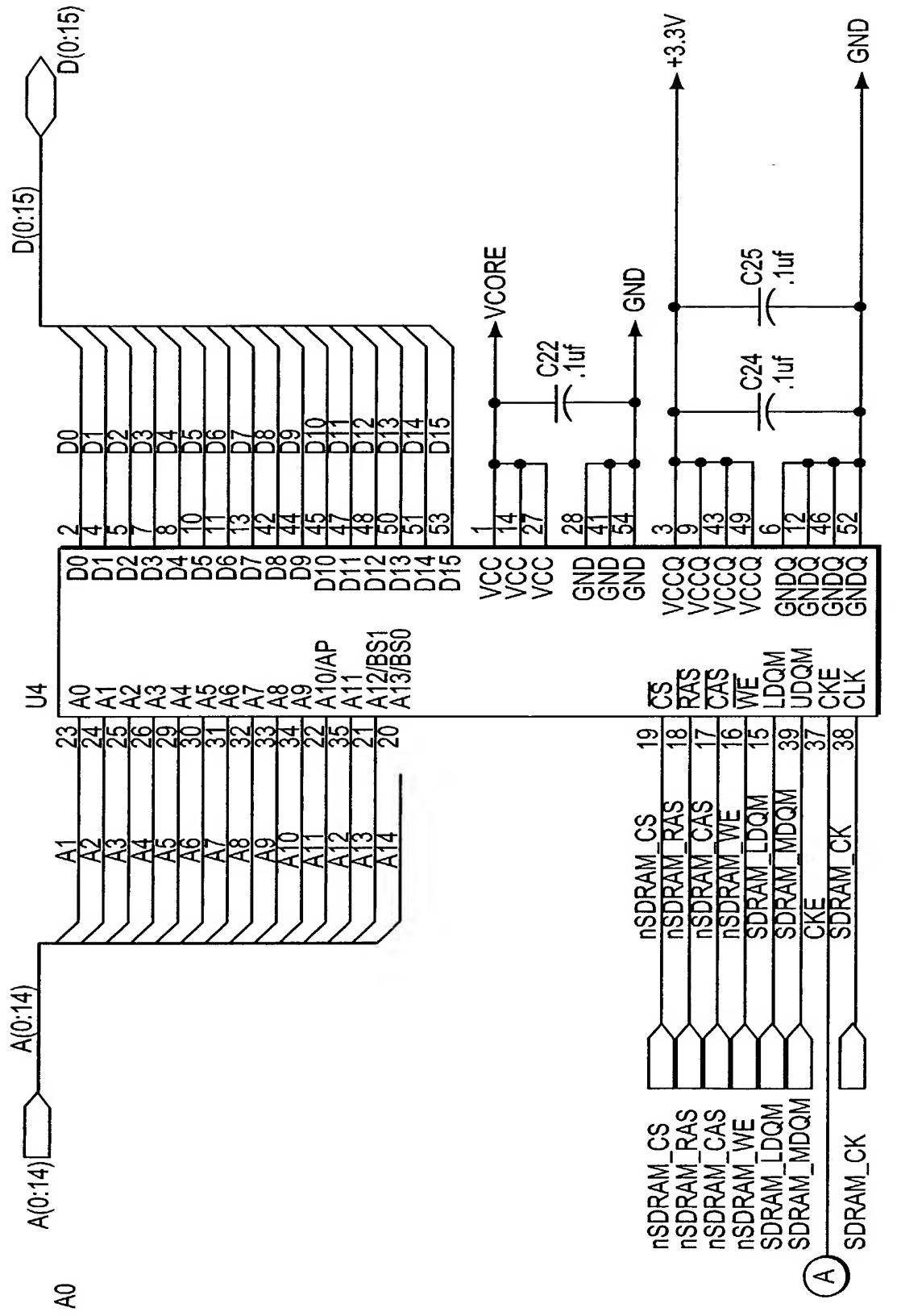


FIG. 6B 4M x 16 SDRAM SHOWN, CAN ALSO USE 1M x 16 WITHIN THE SAME FOOTPRINT.

NOTE: THIS DESIGN REQUIRES SDRAM PARTS WITH ISOLATED Vcc AND VccQ ON CHIP.

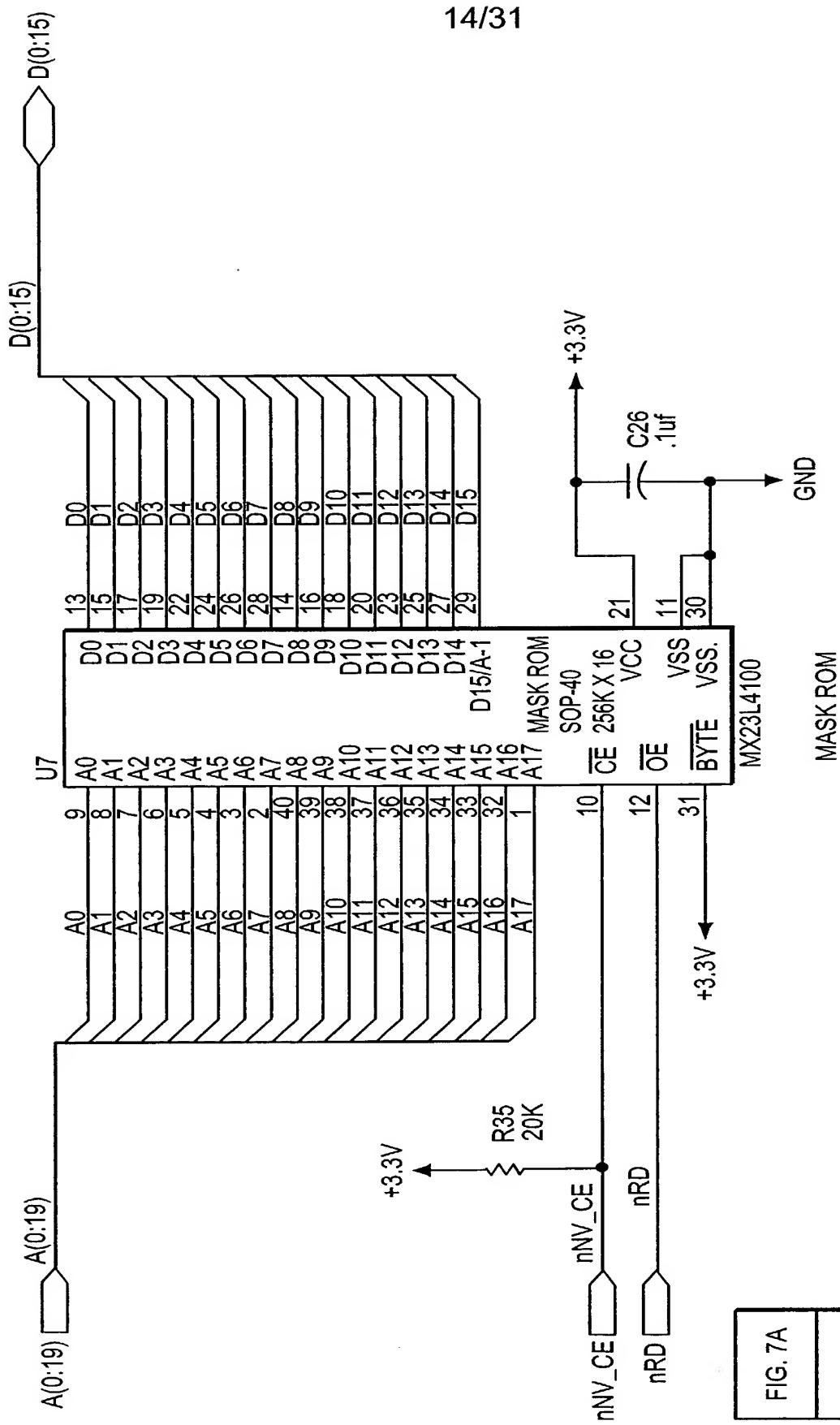


FIG. 7

FIG. 7A

FIG. 7B

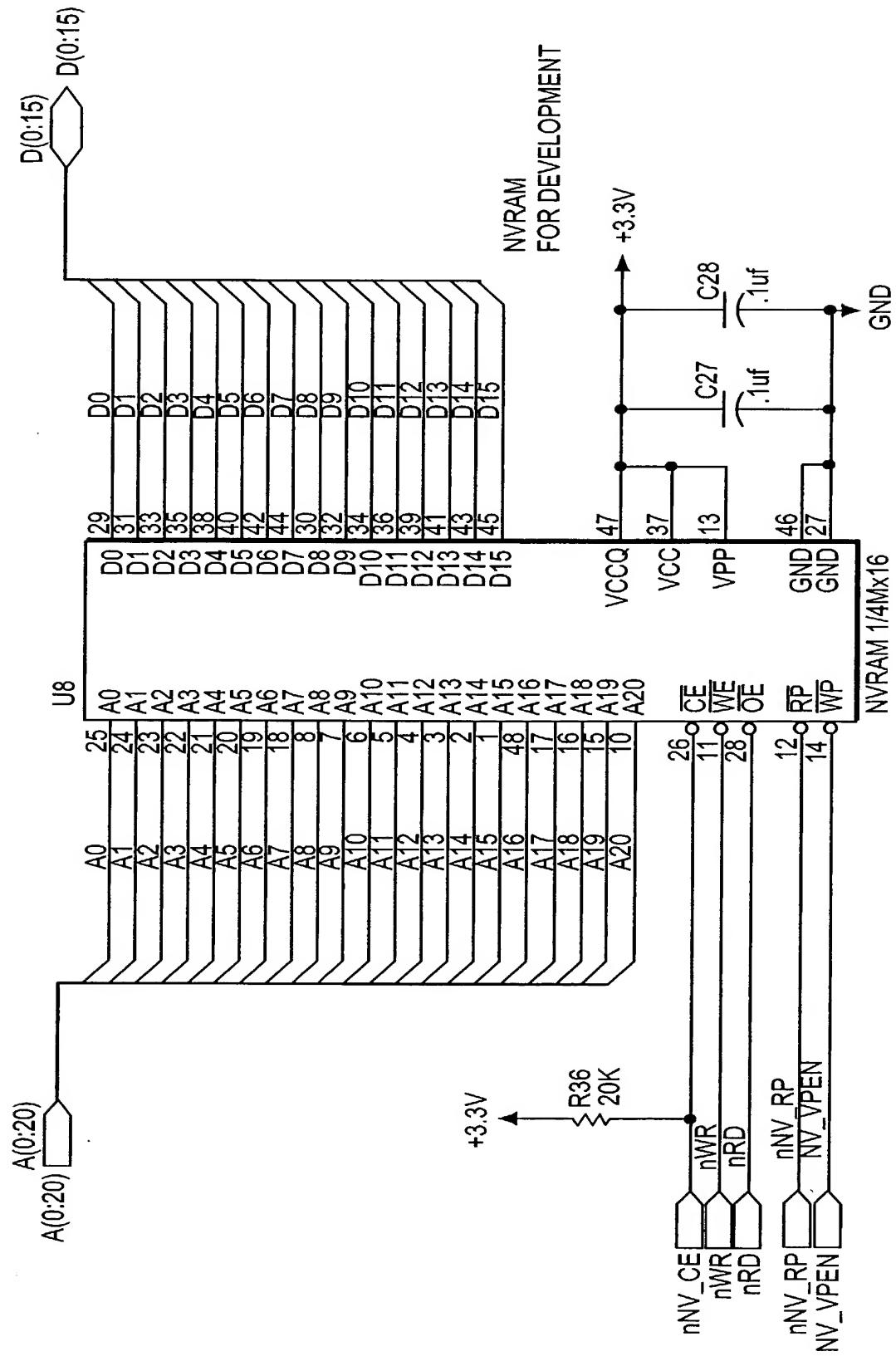


FIG. 7B

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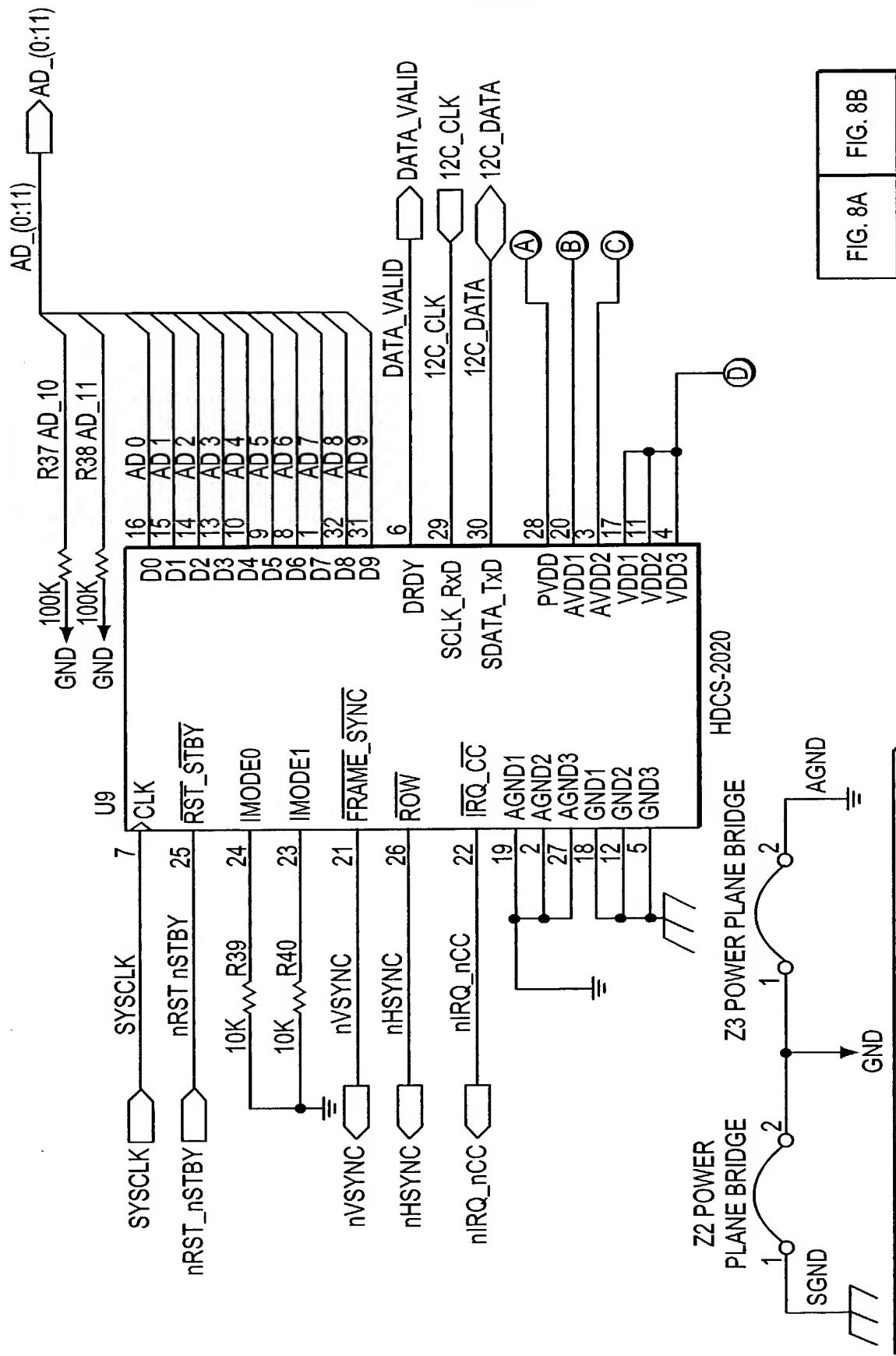


FIG. 8

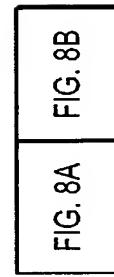
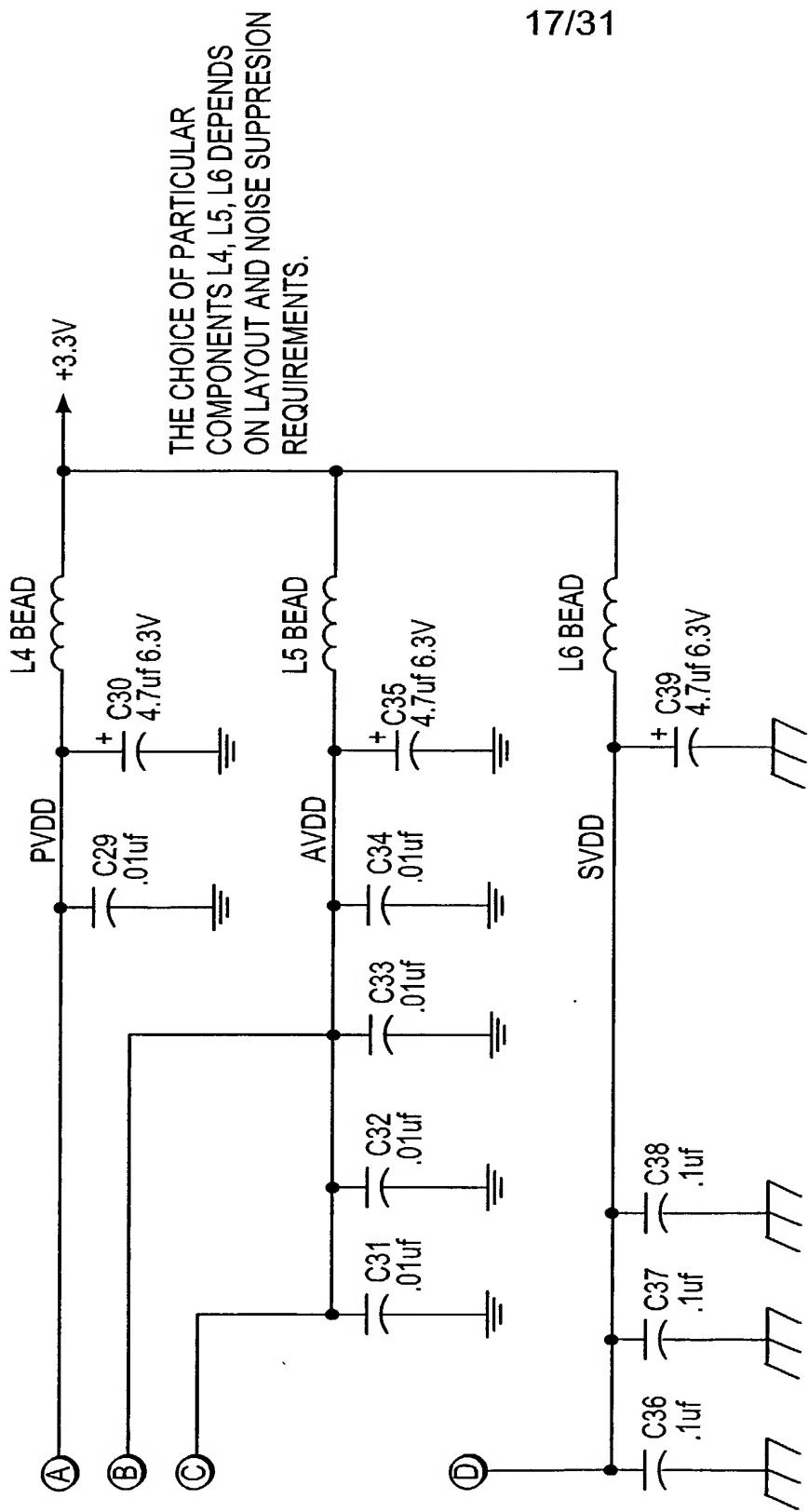


FIG. 8A

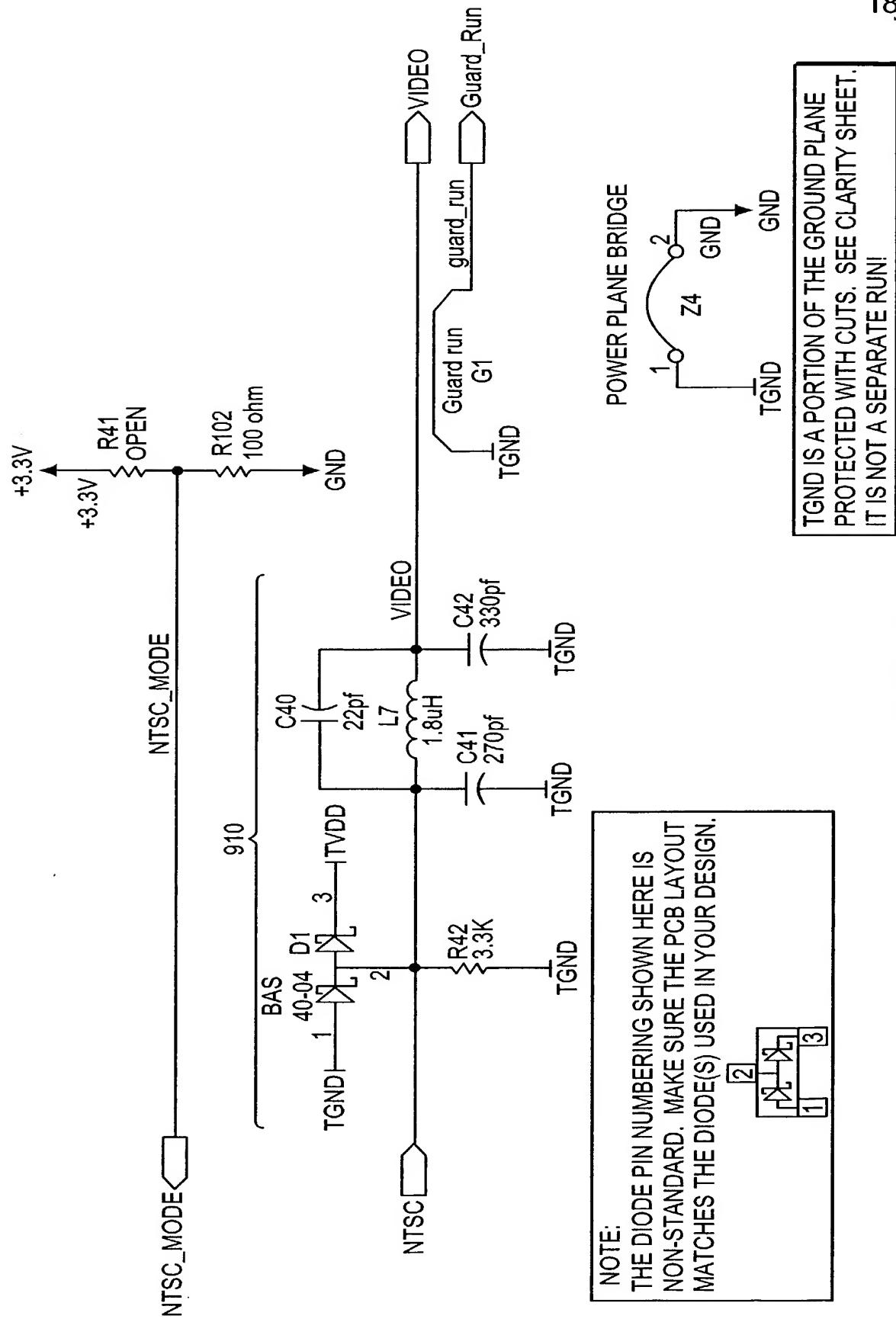
Z2 POWER PLANE BRIDGE
Z3 POWER PLANE BRIDGE
AGND AND SGND ARE PORTIONS OF THE GROUND PLANE
PROTECTED WITH CUTS.
THEY ARE NOT SEPARATE RUNS!

FIG. 8A



PLACE THESE CAPACITORS AND INDUCTORS (BEADS) AS CLOSE AS POSSIBLE TO THEIR RELEVANT PINS ON THE SENSOR PACKAGE. THIS GENERALLY REQUIRES MOUNTING THESE PARTS ON THE BACK OF THE BOARD BEHIND THE SENSOR TO ALLOW LENS MOUNTING. DOUBLE UP VIAS WHERE POSSIBLE, ESPECIALLY THE GROUND PLANE CONNECTIONS.

FIG. 8B

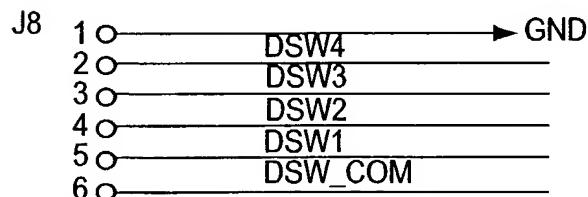
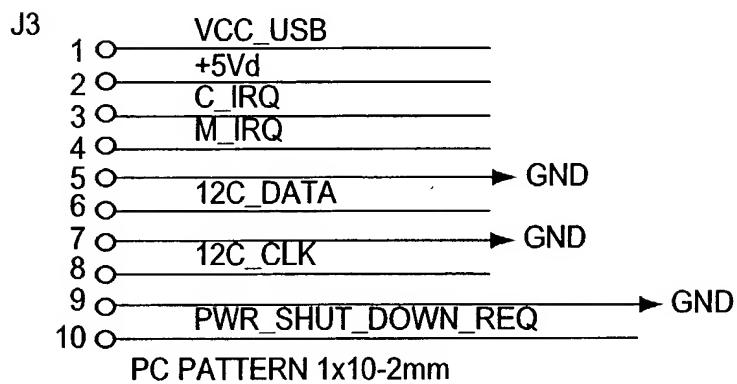
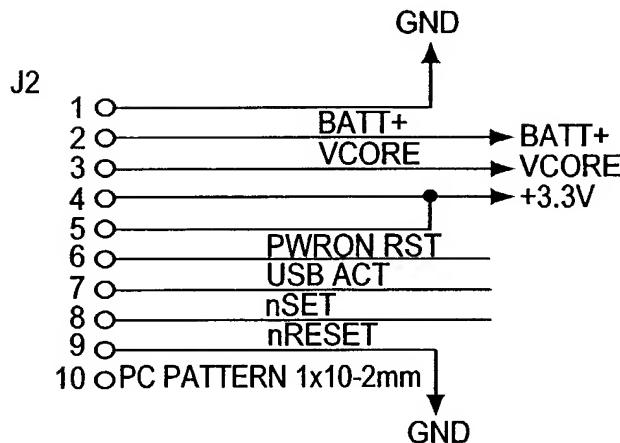


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FIG. 10A FIG. 10B

FIG. 10

MAIN BOARD CONNECTIONS



NOTE:

USE VERY WIDE TRACES FOR BATT+, +5Vd,
VCORE, VBB AND THE +3.3V POWER PATH,
PREFERABLY ON A POWER PLANE

FIG. 10A

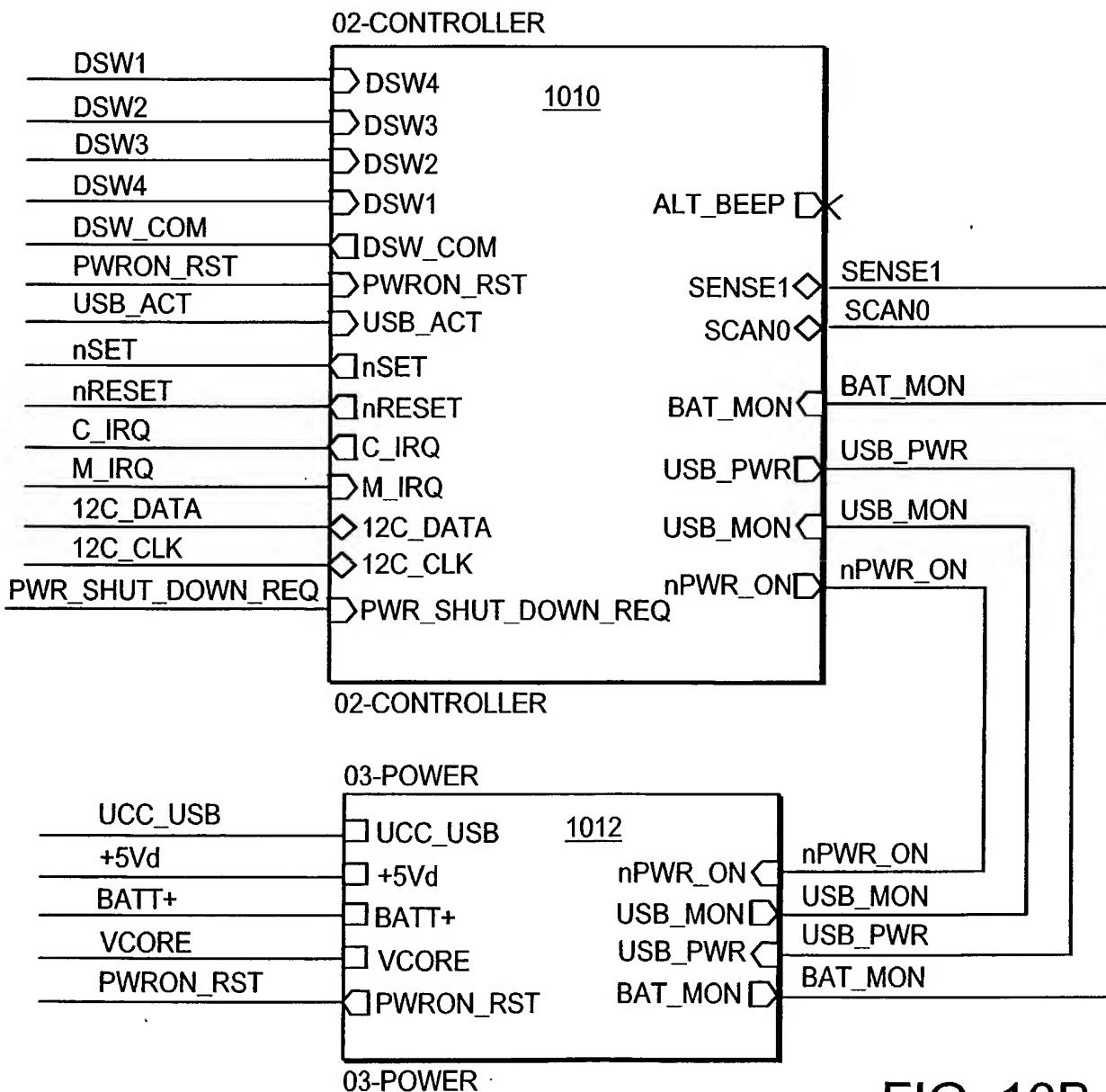
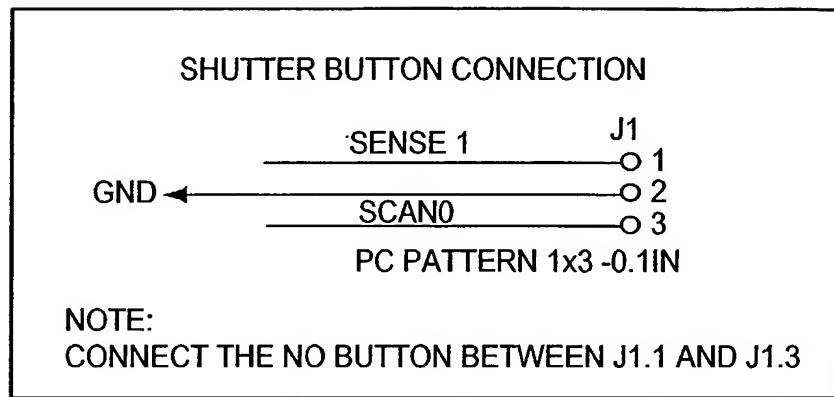
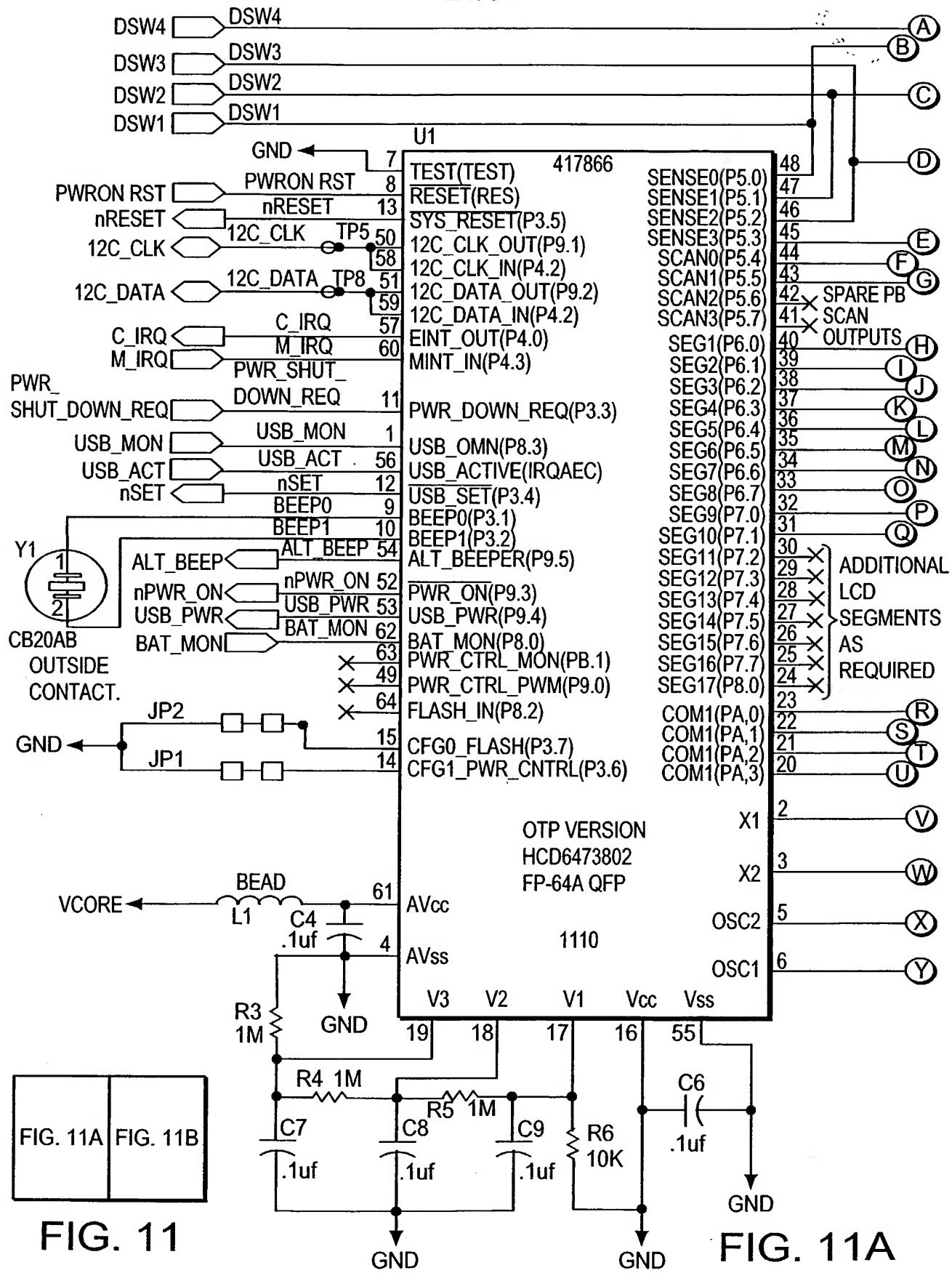
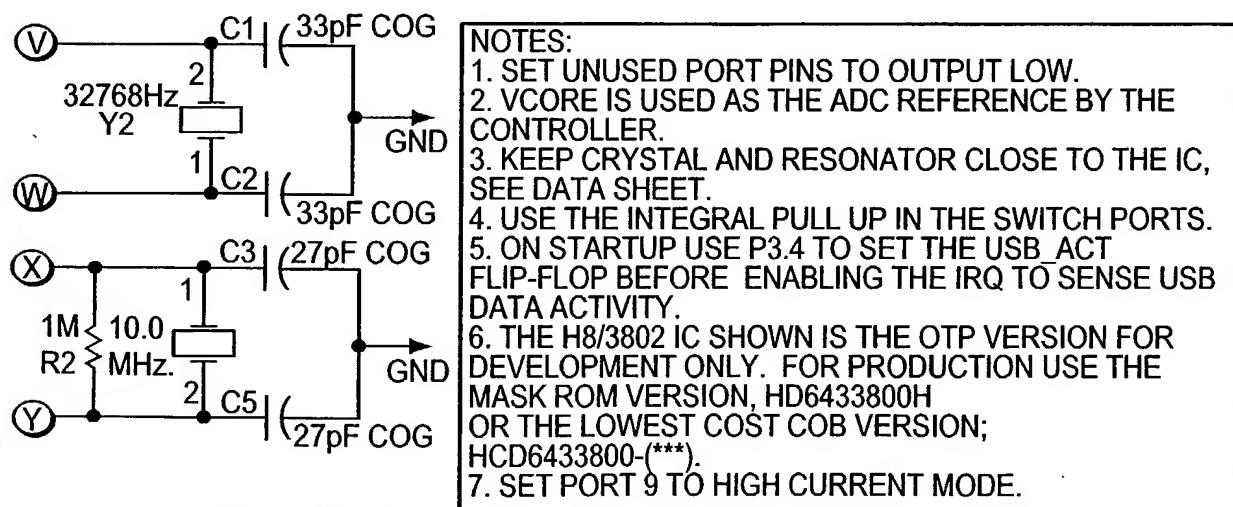
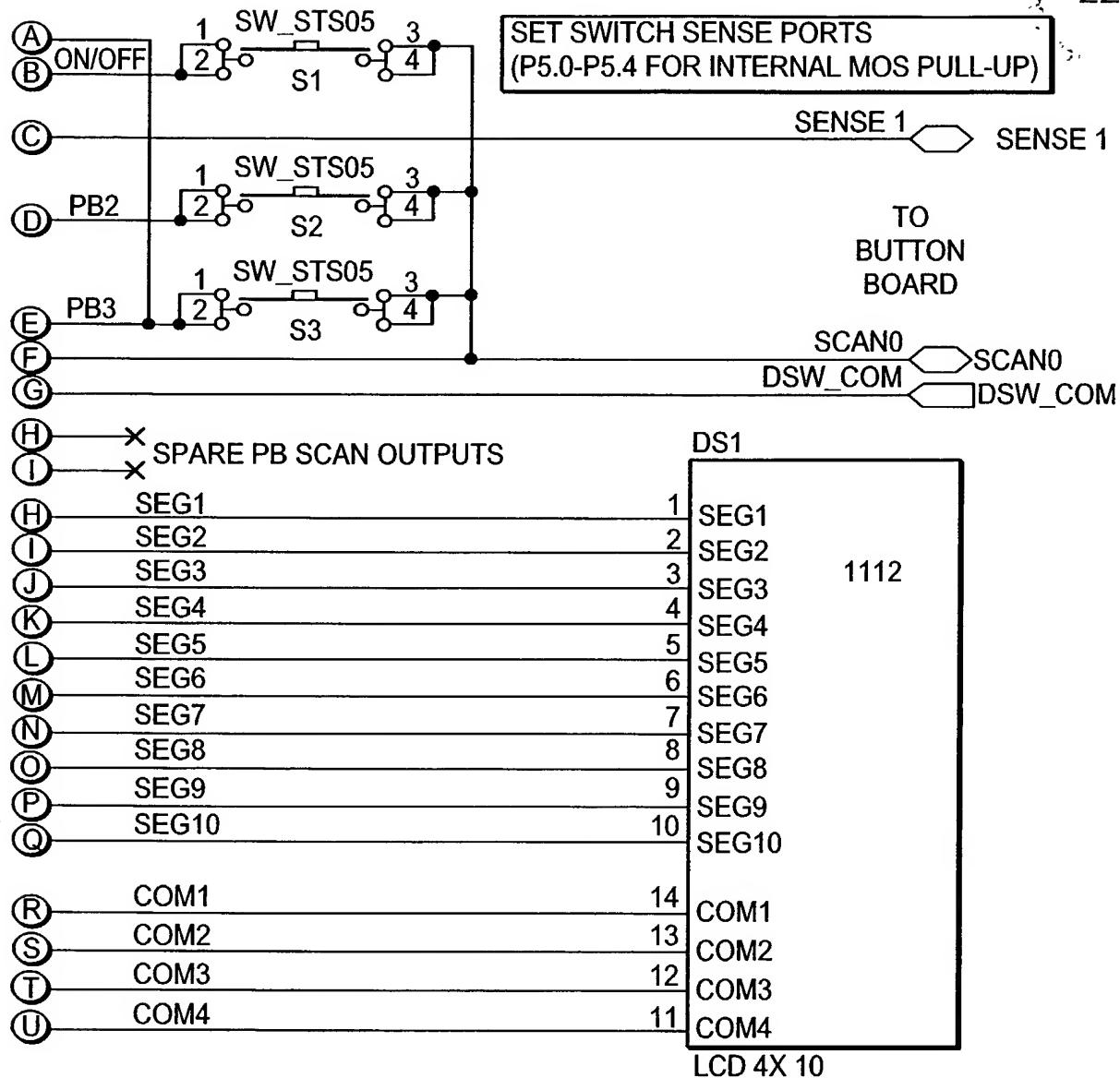


FIG. 10B

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**FIG. 11B**

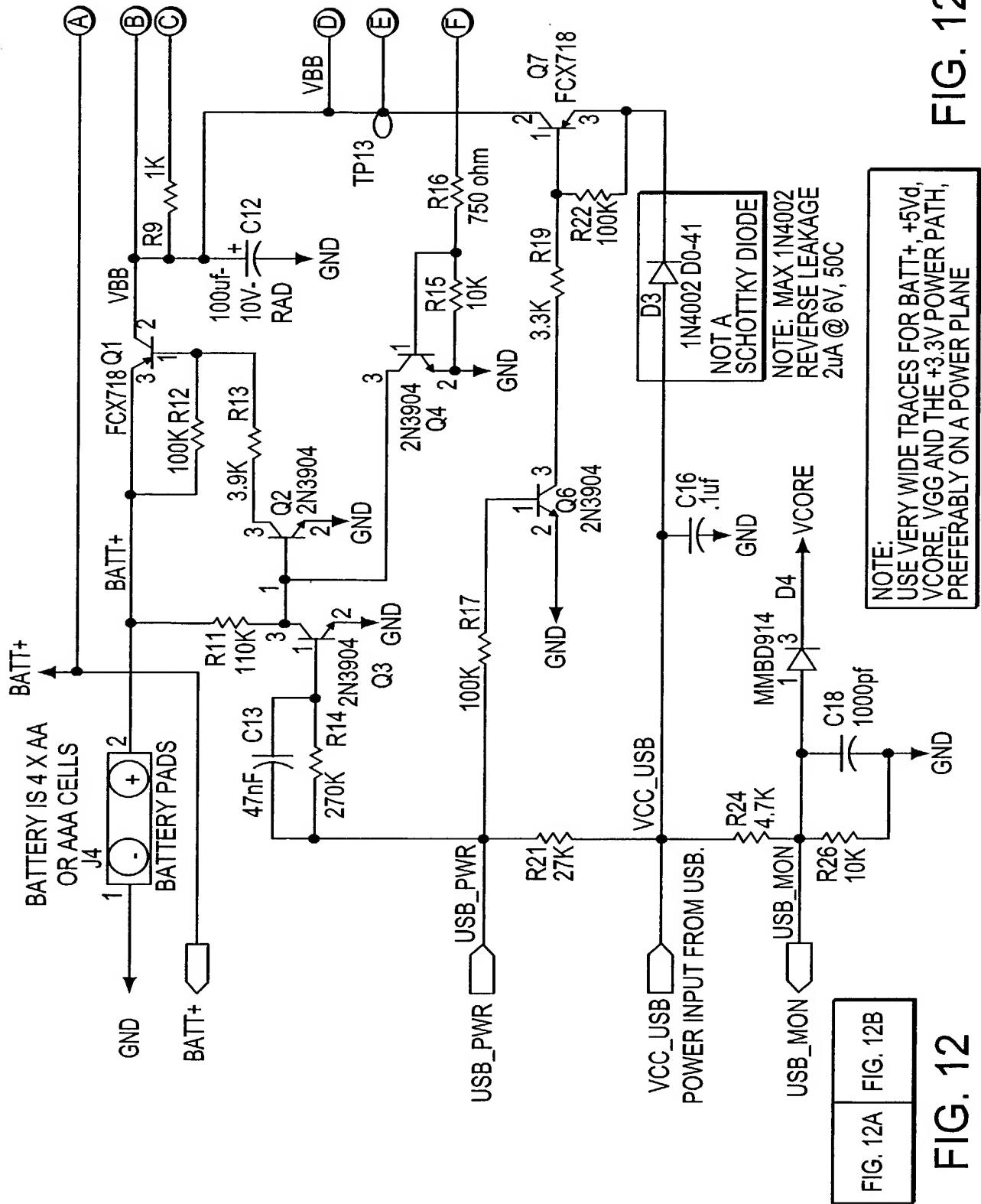


FIG. 12

FIG. 12A

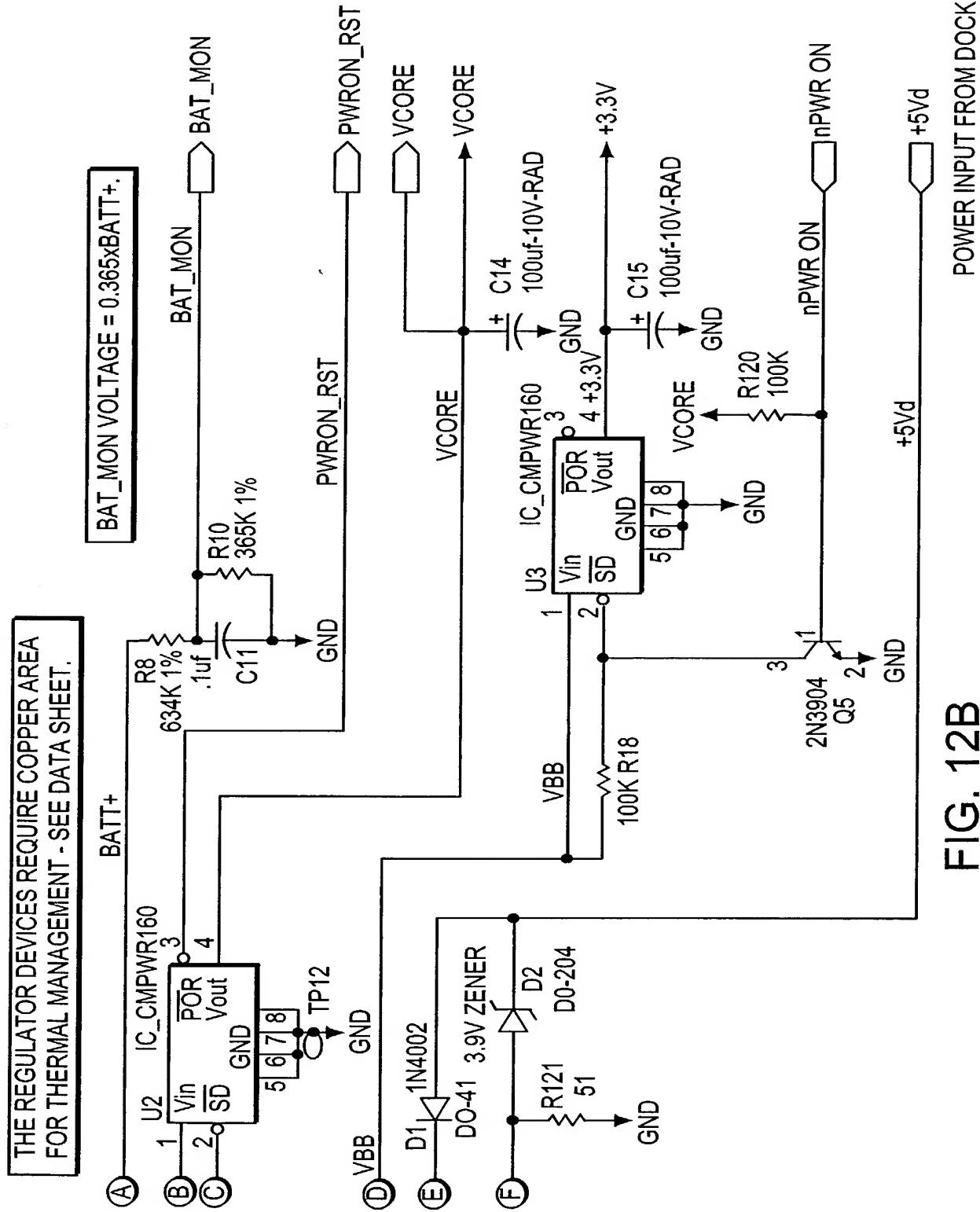


FIG. 12B

POWER INPUT FROM DOCK.

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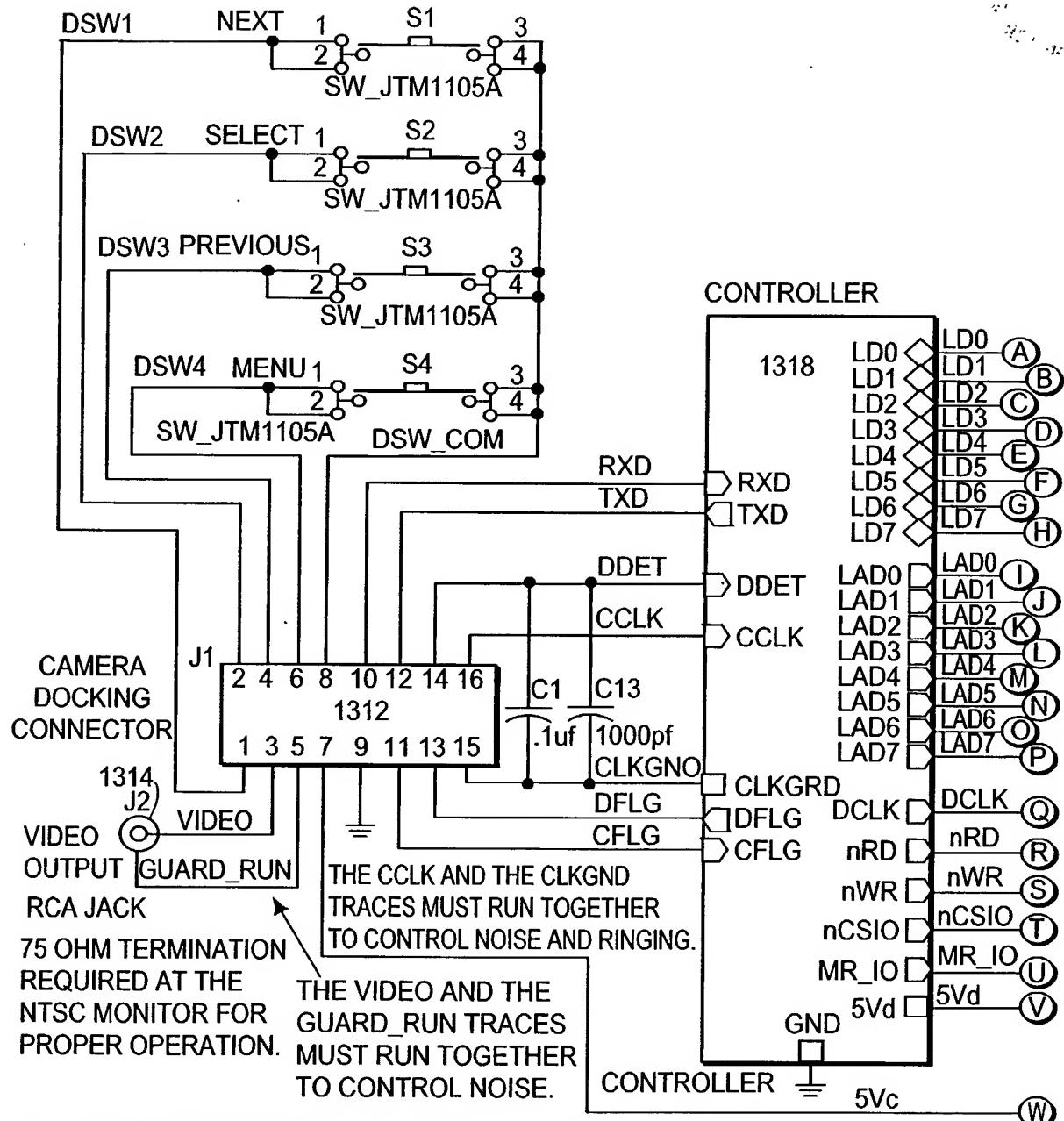


FIG. 13A FIG. 13B

FIG. 13

FIG. 13A

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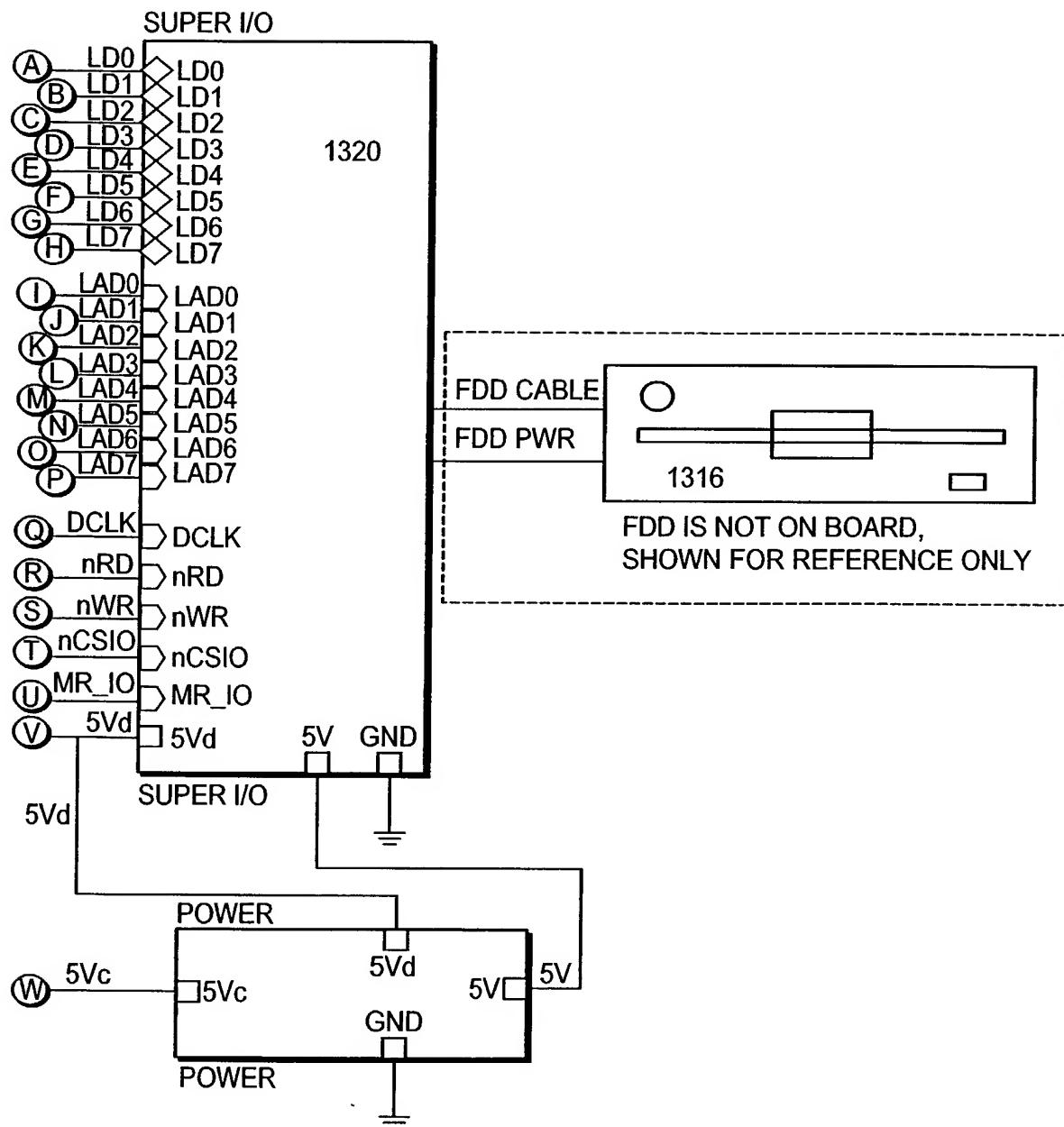


FIG. 13B

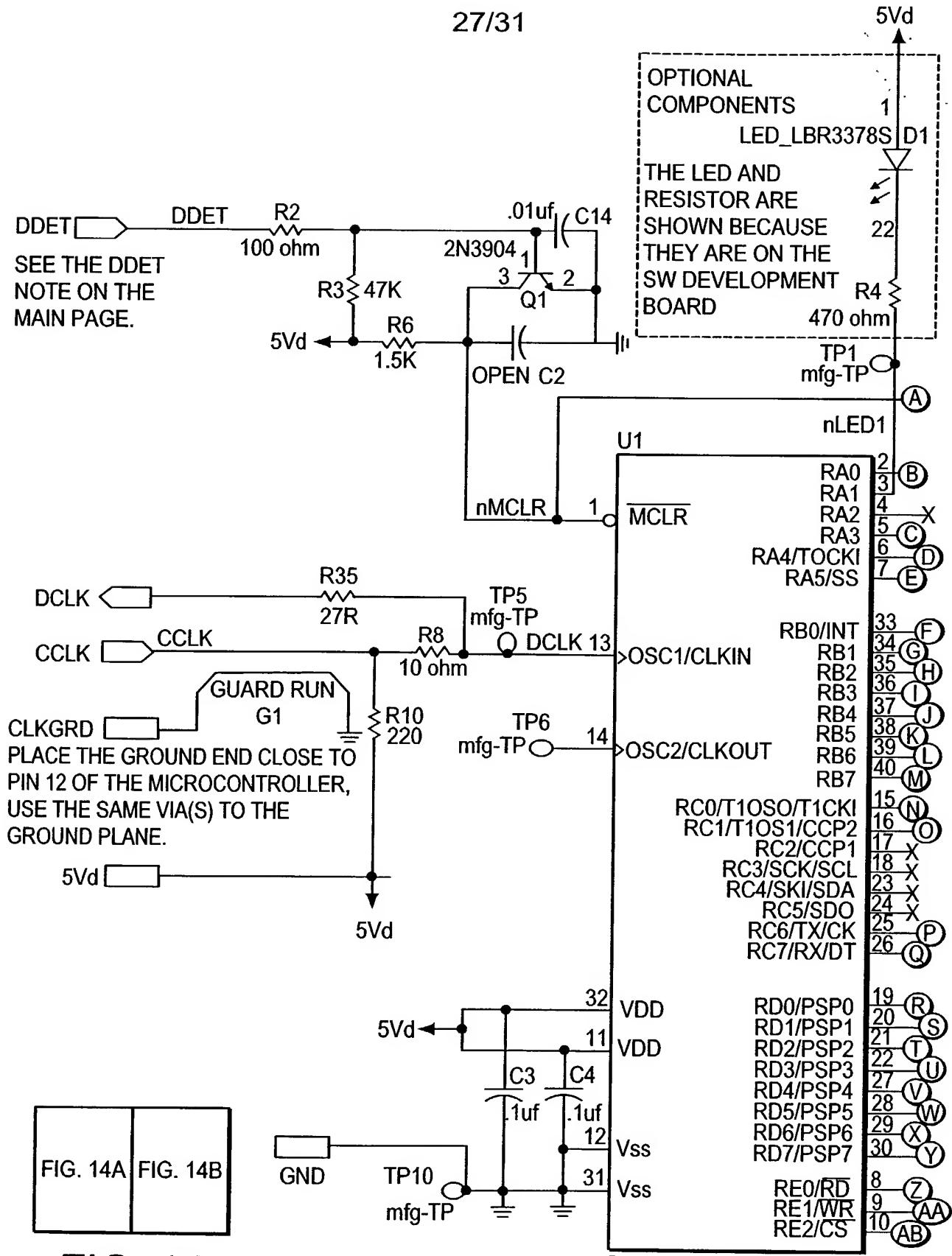


FIG. 14

FIG. 14A

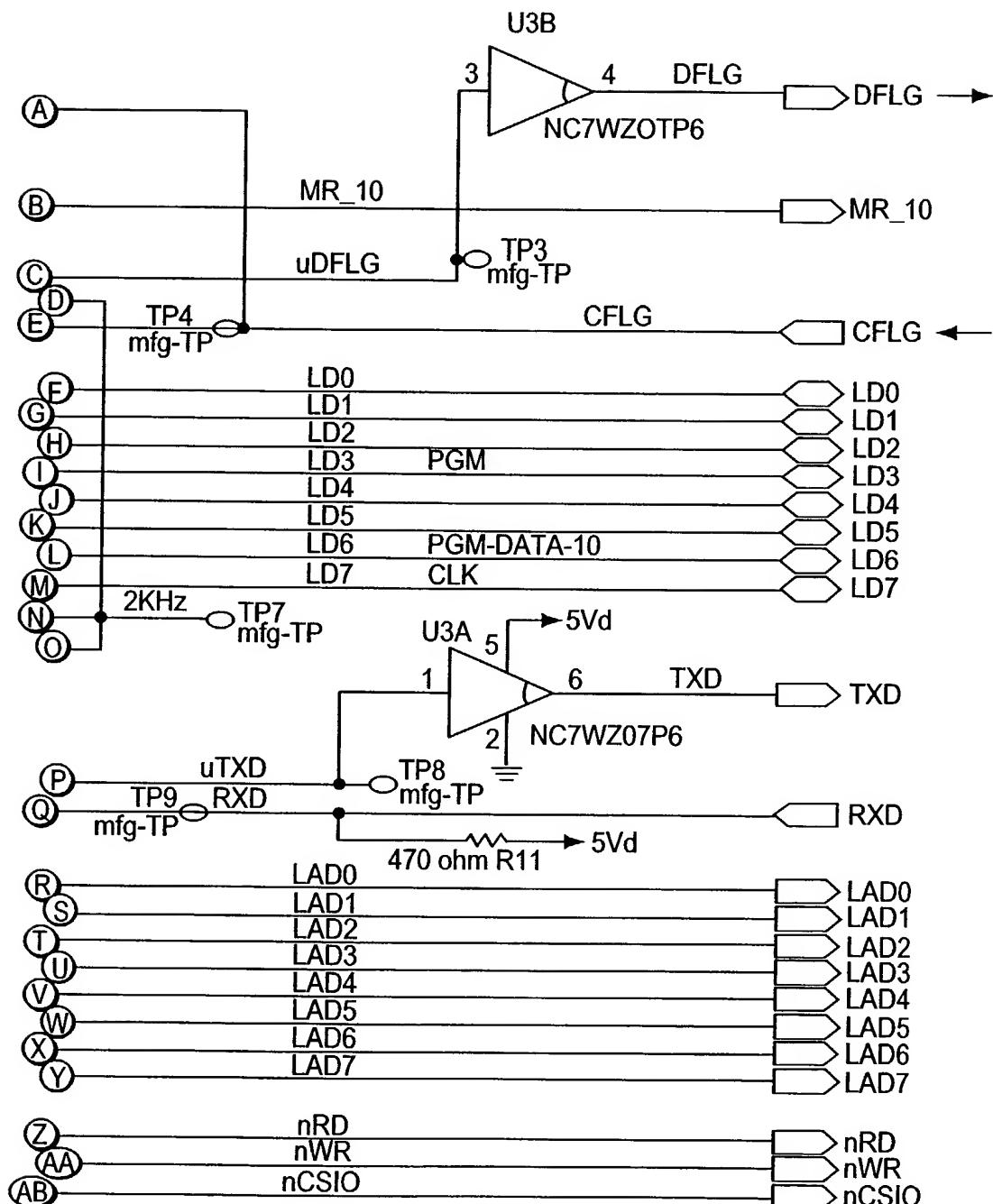
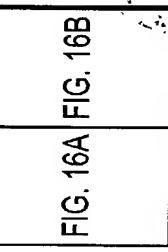
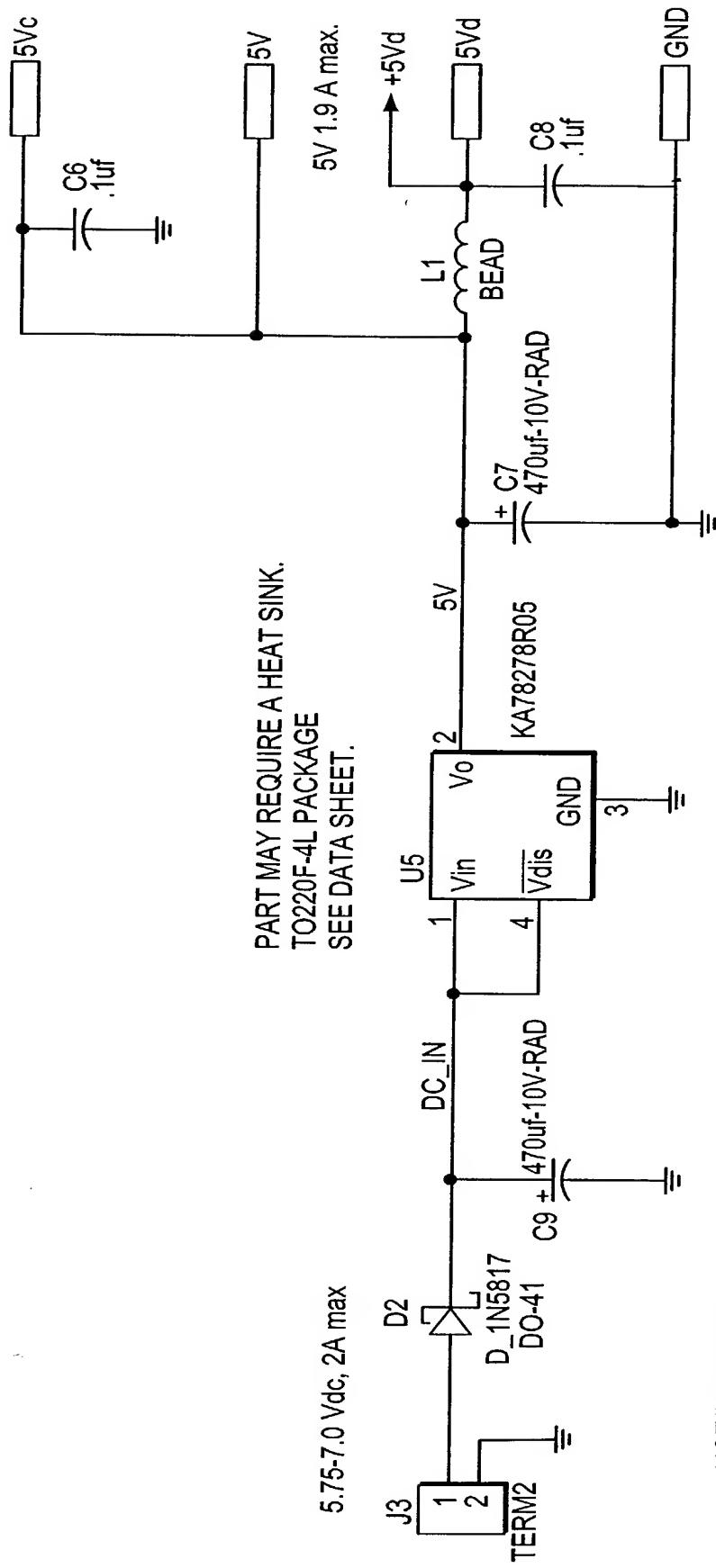
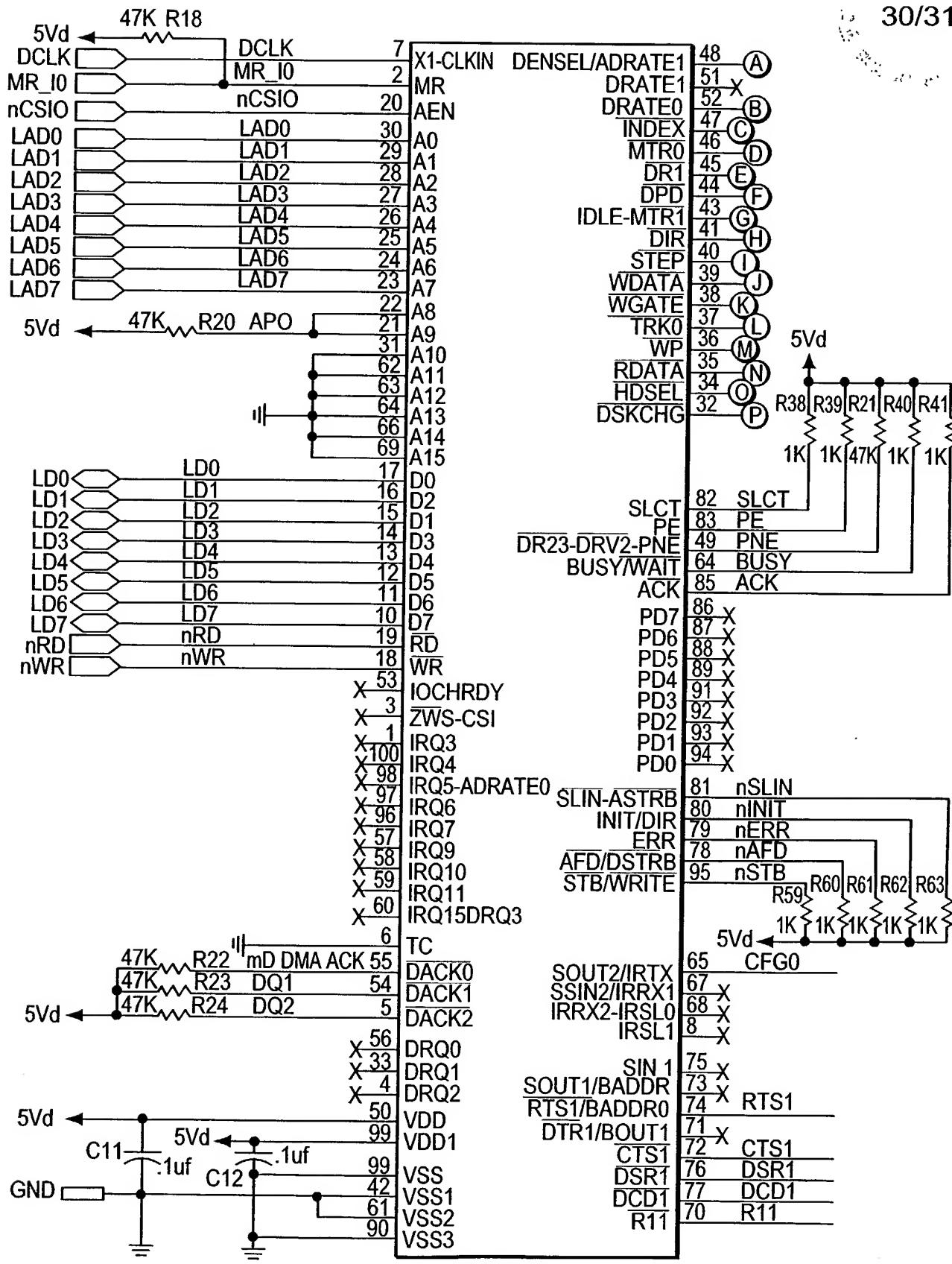


FIG. 14B

**FIG. 16****FIG. 15**



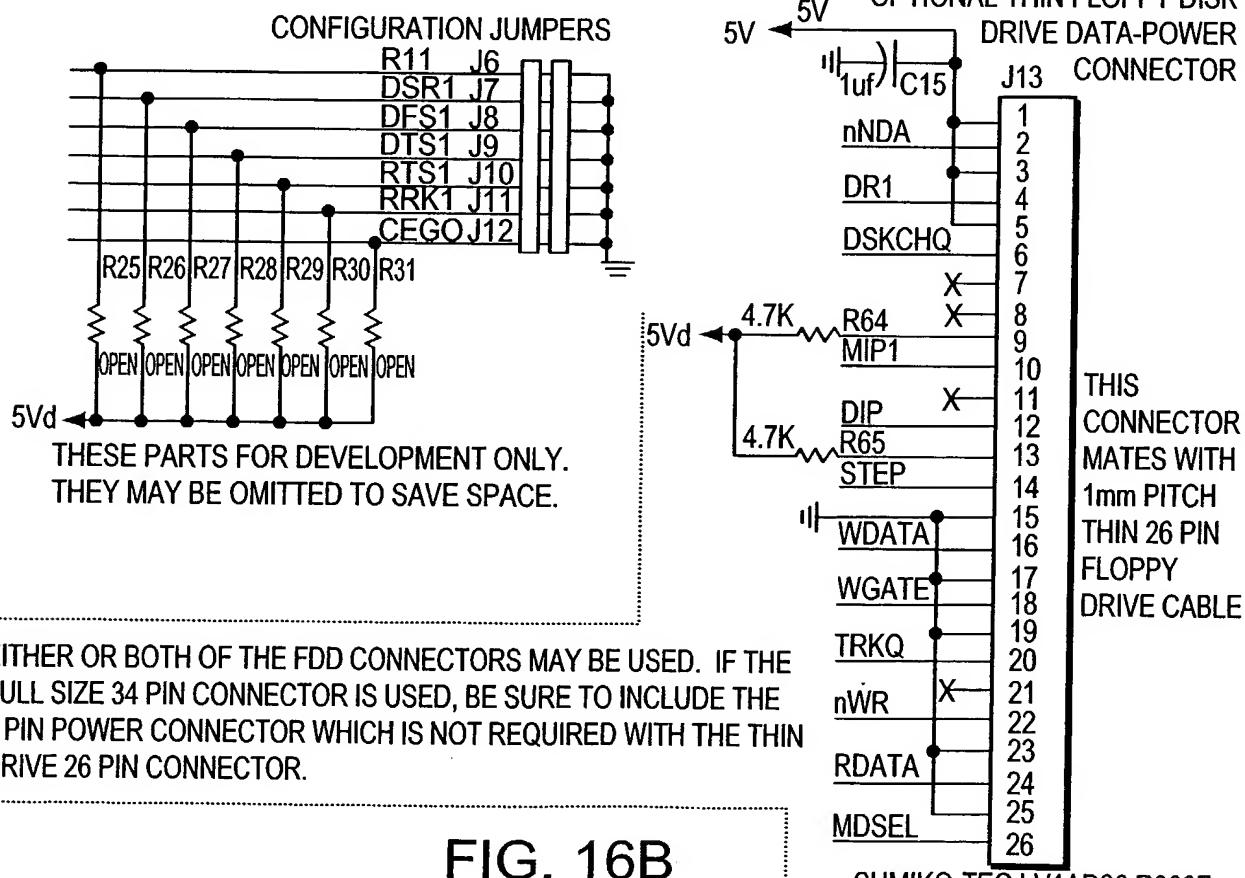
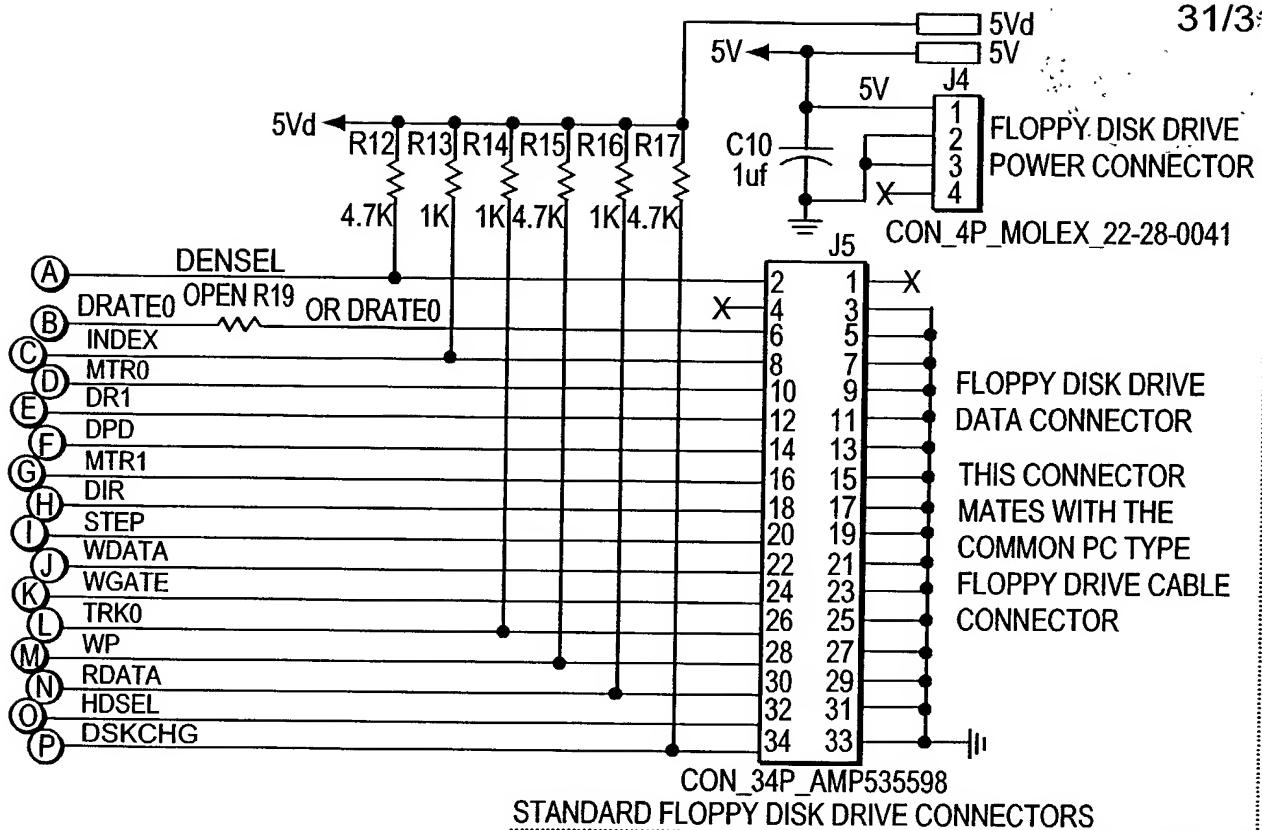


FIG. 16B